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Jury Member Report – Doctor of Philosophy thesis.

Name of Candidate: Fernando Davalos Hernandes

PhD Program: Engineering Systems

Title of Thesis: Supercapacitor Energy Storage System based on Modular Multilevel Converter with embedded self-balance control

Supervisor: Associate Professor Federico Martin Ibanez

Name of the Reviewer: Vedran Perić

I confirm the absence of any conflict of interest	**Date: 14-08-2023**

The purpose of this report is to obtain an independent review from the members of PhD defense Jury before the thesis defense. The members of PhD defense Jury are asked to submit signed copy of the report at least 30 days prior the thesis defense. The Reviewers are asked to bring a copy of the completed report to the thesis defense and to discuss the contents of each report with each other before the thesis defense.

If the reviewers have any queries about the thesis which they wish to raise in advance, please contact the Chair of the Jury.

Reviewer's Report

Reviewers report should contain the following items:

- Brief evaluation of the thesis quality and overall structure of the dissertation.
- The relevance of the topic of dissertation work to its actual content
- The relevance of the methods used in the dissertation
- The scientific significance of the results obtained and their compliance with the international level and current state of the art
- The relevance of the obtained results to applications (if applicable)
- The quality of publications

The summary of issues to be addressed before/during the thesis defense

- ***Brief evaluation of the thesis quality and overall structure of the dissertation***

The thesis provides a contribution to the domain of power electronics by providing a detailed design of a MMC converter to be used with a supercapacitor energy storage. The proposed MMC topology has several advantages. The best quality of the thesis lies in the detailed assessment of the proposed topology and its experimental validation. From the structure point of view, the thesis provides all necessary details, but it can also be improved in the sense that the main novelty of the thesis comes relatively late in the manuscript (after roughly 50% of the text). I would recommend considering moving a lot of literature review from the beginning, where the operation of conventional topologies is described, to the appendix, as this material is known and just puts additional burden to understanding the main contribution of the thesis. In addition, a lot of text goes to the context, which is in my view not necessary for the thesis and spoils the flow of reading. For example thermal energy storage description is not relevant for this work. In addition, the issues bulk power systems are facing are too extensively discussed.

- ***The relevance of the topic of dissertation work to its actual content***

The MMC converters are gaining popularity in different application areas, which makes this thesis very topical. The proposed topology is modular thanks to the incorporating several functions such as balancing, conversion and energy storage in a single submodule. In this regard, the thesis provides the contribution according to the international standards. The presented work may lead to the further research where the proposed topology might find application where conventual converters are currently used.

- ***The relevance of the methods used in the dissertation***

The experimental development and the level of detail in assessing the performance of the proposed topology is especially to be commended. Therefore, the approach and methods used are suitable for a PhD thesis. Moreover, the thesis can serve as an example how the performance of the new power electronics topologies should be assessed.

- ***The scientific significance of the results obtained and their compliance with the international level and current state of the art***

The thesis presents sufficient level of novelty according to the international standards. The state of the art is very well described in the thesis (as mentioned before maybe even too extensive), however it shows that the candidate has the good understanding of the current challenges in designing power electronic converters.

- ***The relevance of the obtained results to applications (if applicable)***

The obtained performances in terms of the efficiency of the converter are convincing and aligned with the best practices in the domain, which makes the proposed topology a potentially interesting for several future applications.

- ***The quality of publications***

The thesis results have been published in 4 publications, of which are two international journals (Energies and IEEE Access) and two internationally renowned conferences (IECON and EPE ECCE). The named journals belong to the second tier of the most renowned journals in the field and therefore, the candidate's publication record is sufficient for the successful defense of the thesis.

Provisional Recommendation

☒ *I recommend that the candidate should defend the thesis by means of a formal thesis defense*
☐ *I recommend that the candidate should defend the thesis by means of a formal thesis defense only after appropriate changes would be introduced in candidate's thesis according to the recommendations of the present report*
☐ *The thesis is not acceptable and I recommend that the candidate be exempt from the formal thesis defense*

Skoltech
Skolkovo Institute of Science and Technology

Supercapacitor Energy Storage System based on Modular Multilevel Converter with embedded self-balance control

Doctoral Thesis
by

Fernando Dávalos Hernández

Doctoral Program in Engineering Systems

Supervisor
Associate Professor Federico Martin Ibañez

Moscow 2023

I hereby declare that the work presented in this thesis was carried out by myself at Skolkovo Institute of Science and Technology, Moscow, except where due acknowledgement is made and has not been submitted for any other degree.

Fernando Dávalos Hernández

Associate Prof. Federico Martin Ibañez

Abstract

As renewable energy sources interconnected to the grid increase, a viable solution to sustain the stability of the grid is by deploying distributed Energy Storage Systems (ESS) along the grid. For this application, ESSs should be capable of managing high-power ratings in milliseconds to seconds time range, thus Supercapacitors (SCs) are attractive devices to fulfill this requirement. The research objective is to design an ESS topology that can be expandable and scalable, avoiding the complexity of actual systems by adopting the Modular Multilevel Converter (MMC) approach. For this reason, an important aspect is to enhance the submodules with self-balancing capabilities to accommodate as many SCs as required by the grid application.

MMCs have been deeply studied for high-voltage DC applications, although an expensive technology, the benefits for implementing it in large-scale projects turn them a viable solution in contrast with traditional AC lines, as they provide a more robust and efficient way to transfer energy in long distances. Few research has been done in low-voltage MMC applications due the complexity of the controller and the limited benefits in efficiency, but it is an innovative approach to add to each Submodule (SM) an energy storage device to create ESS. The resulting ESS can scale more quicker as it is possible to just add more SMs to the system in series to increase the voltage or in parallel to increase the power. In addition, with the added capability to self-balance the SCs, a robust ESS can be designed in comparison to traditional ones which requires independent power

You should advertise more your work in abstract, what you have done, which problem you have solved, how, and why your work is important and not just give the general problems

stages to accomplish the balancing system, the DC/DC converter, and the DC/AC inverter.

In line with the mission of the Center of Energy and Technology at Skoltech, this research in energy conversion can provide a cost-efficient ESS converter and it can be used to enhance frequency control capabilities of the grid. To conclude, a relevant contribution in the field of low-voltage MMC was made with this PhD research work.

Publications

1. **Hernandez, Fernando Davalos**, Federico Ibanez, Sebastian Gutierrez, and Wilmar Martinez. 2020. “Improvements on Signal-to-Noise Ratio in Feedback Measurement in DC/DC Converters.” In *2020 22nd European Conference on Power Electronics and Applications, EPE 2020 ECCE Europe*. Institute of Electrical and Electronics Engineers Inc. doi:10.23919/EPE20ECCEEurope43536.2020.9215774.

2. **Hernandez, Fernando Davalos**, Federico Ibanez, Rahim Samanbakhsh, and Ramiro Velazquez. 2021. “A Comparative Study of Energy Storage Systems Based on Modular Multilevel Converters.” In IECON Proceedings (Industrial Electronics Conference). Vol. 2021-October. IEEE Computer Society. doi:10.1109/IECON48115.2021.9589539.

3. **Davalos Hernandez, Fernando**, Rahim Samanbakhsh, Parham Mohammadi, and Federico Martin Ibanez. 2021. “A Dual-Input High-Gain Bidirectional DC/DC Converter for Hybrid Energy Storage Systems in DC Grid Applications.” *IEEE Access* 9. Institute of Electrical and Electronics Engineers Inc.: 164006–16. doi:10.1109/ACCESS.2021.3132896.

4. **Hernandez, Fernando Davalos**, Rahim Samanbakhsh, Federico Martin Ibanez, and Fernando Martin. 2022. “Self-Balancing Supercapacitor Energy Storage System Based on a Modular Multilevel Converter.” *Energies* 15 (1). MDPI. doi:10.3390/en15010338.

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To my supervisor who always encouraged me to work beyond the difficulties of the pandemic, for giving me all its expertise in power electronics, and for truthfully believing in my research.

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To my family for always supporting and encourage me to pursue greater goals.

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1. Introduction

In 2019 the renewable energy generation expanded more than electricity demand, resulting in a decrease in fossil-fuel electricity generation, achieving a never-seen scenario [1]. Even though we are facing the post-pandemic economic havoc that Covid-19 let us, we must continue supporting the integration of renewables to the grid globally. The tendency to increase annual renewable capacity additions is an encouraging development [2], but it is not enough to reduce our dependency on fossil fuels and control CO_2 emissions. As Fig. 1 shows the International Renewable Energy Agency (IRENA) forecast and required future scenarios in fossil-fuel energy demand.

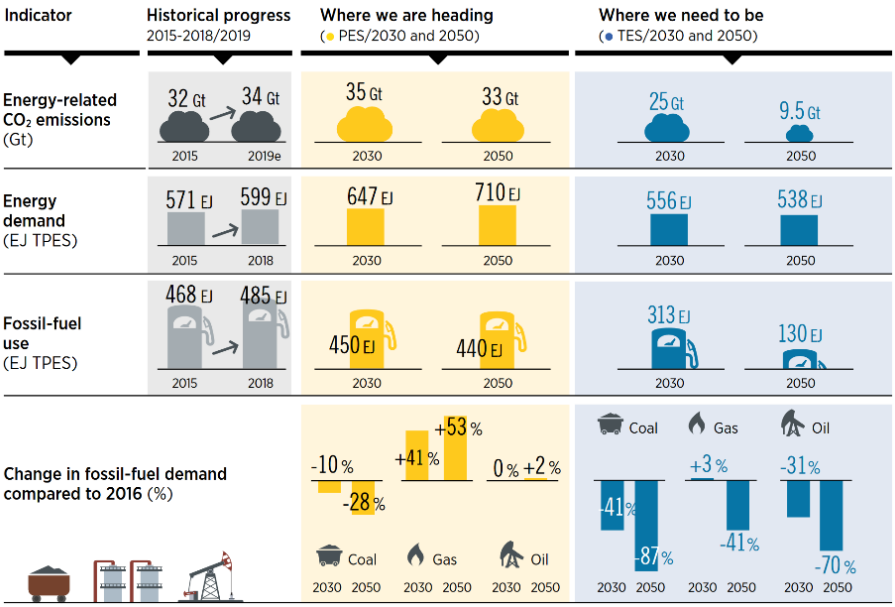


Fig. 1 IRINA's forecast for fossil-fuel energy demand and CO_2 emissions [1].

To meet Paris agreements of reducing by 70% the carbon emissions and by 64% the demand of fossil fuels, renewable energy among solar and wind are the more promising ones. However, they come with a challenge for the electric energy industry,

their stochastic behavior. For this reason, several new technologies have to be developed, including electricity storage, namely Energy Storage Systems (ESSs), electric vehicles, smart appliances and meters [1], [3].

1.1. Why ESS are needed, application examples

ESSs will become a standard for any grid operator since these types of systems would allow the further integration of Variable Renewable Energy (VRE). For today's standards FACTS devices are widely implemented by grid operators to extend and increase the power transfer capability of the transmission lines and provide a stable supply for the consumers. ESSs are the evolution of the STATCOM FACT devices by allowing a bigger shift in time or capacity of the generated power when required, and still maintain a stable supply for the consumers [4].

Therefore, the grid will require the addition of the ESSs at different points of the grid, for example before the transmission lines, through the distribution grid and at the consumer side (residential or commercial) as Fig. 2 illustrates. This will increase the flexibility of the grid and still maintain a stable supply [3], [5], [6].

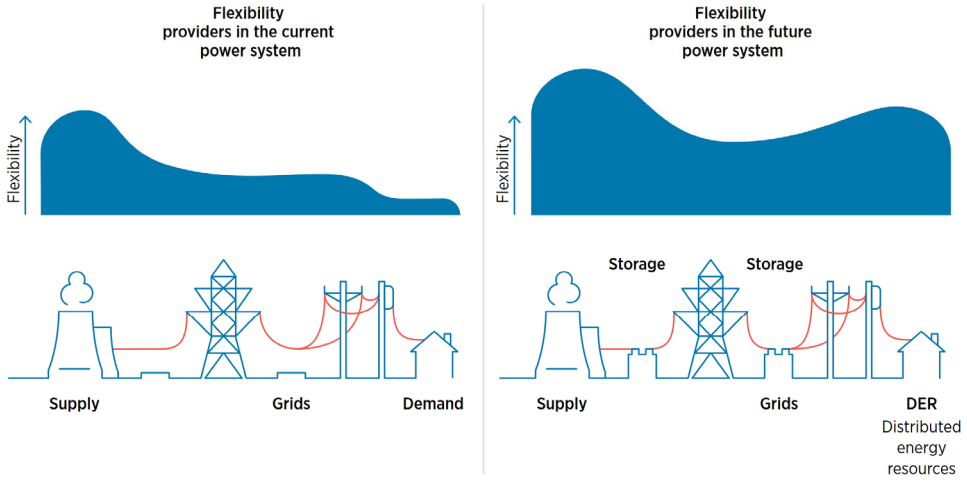


Fig. 2 Traditional grid vs emerging flexible grid [5].

This flexibility cannot be provided by the actual grid due the fact that the generators in the power plants cannot be commanded to abruptly change from delivering full power to zero power or vice versa, as they have slow reaction times and initialization sequences that must be met. ESSs on the other hand can accurately and quickly ramp the power output or absorption and therefore compensate for the deviations in the grid as shown in Fig. 3.

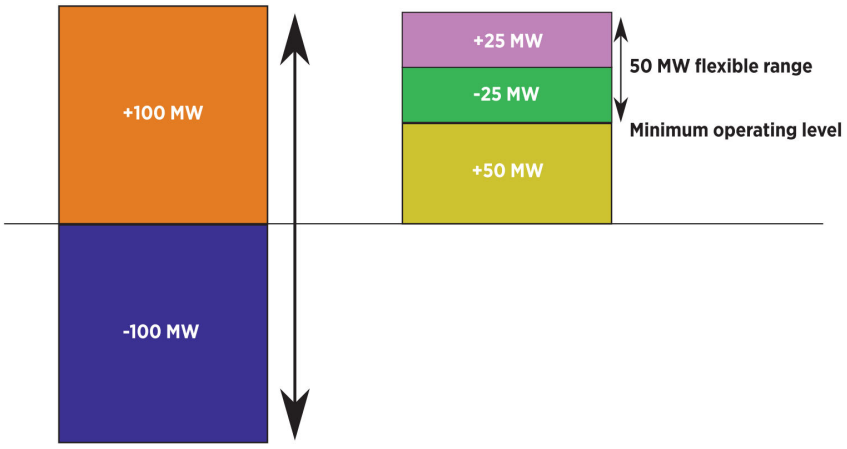


Fig. 3 100MW ESS (left) versus 100MW gas turbine (right) [6].

The power handling capabilities of any ESS is determined by the type of storage device used and the power electronic circuitry. The storage device capacity dictates the time of operation as well as the allowed peak power and most of the cases the circuitry has the same peak power handling capability. Therefore, the design of any ESS is a process that requires to understand the principles of operation of the storage device and optimize the circuitry for it. This thesis's main contributions are in creating an optimized energy conversion circuitry for the ESS.

1.2. Types of energy storage devices and systems

Currently, there are multiple technologies that can provide the required electricity storage. They vary from thermal, electro-mechanical, electro-magnetic and electro-chemical forms.

In the form of thermal storage, the most exploited is molten salt [3], [7]. In the electro-mechanical form, we have two types, Compressed Air Energy Storage (CAES) and flywheels [3], [4], [7]–[9]. In the form of electro-magnetic we have Superconducting Magnetic Energy Storage (SMES) [3], [4], [7], [8]. And finally, in the electro-chemical form of storage we have lithium-ion, sodium-based, redox flow, lead-acid batteries and capacitors and supercapacitors [3], [4], [7]–[10].

There are many parameters involved in the aforementioned energy storage devices, but particularly two of them are relevant when comparing each device is their power density and their energy density. Fig. 4 shows the comparison between the different types of energy storage technologies [3], [4], [7]–[10].

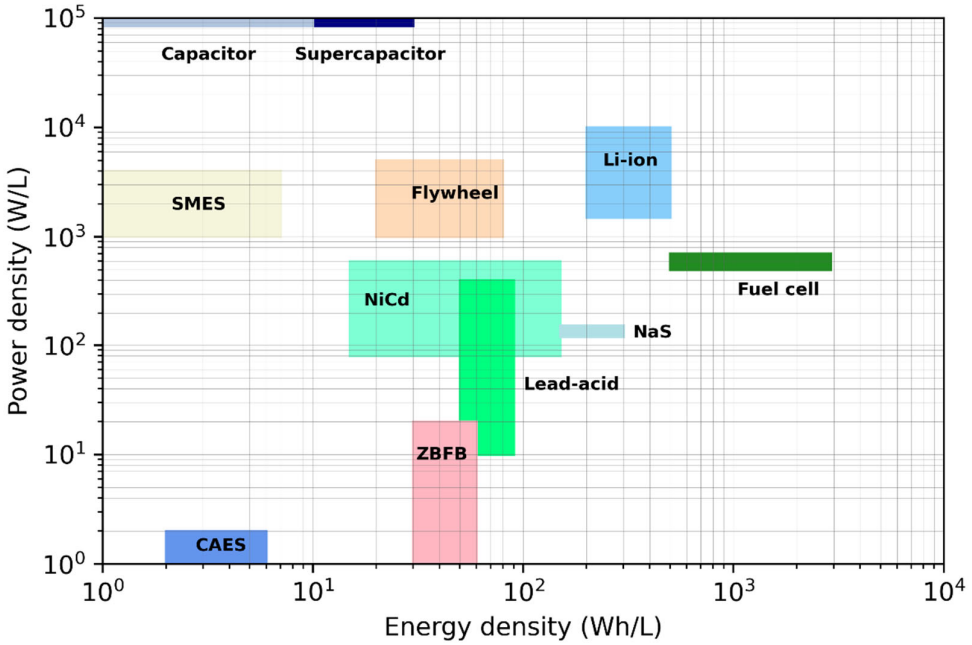


Fig. 4 Energy density and power density comparison between various energy storage devices [3].

Based on Fig. 4 it is possible to infer that if we moved in a diagonal from the left bottom to the upper right the volume would start to decrease, and therefore the technologies that can be found in the corner are the most promising ones. However, other considerations have to be taken into account, like the cost, durability and maintenance.

Depending on the application, the energy storage device must be selected based in a techno-economic analysis that considers all the parameters involved, for such reason there is no ideal energy storage device, and some authors started to analyze the combination of them for creating a hybrid ESS.

IRENA as well as other authors have identified the most suitable energy storage devices based on the application or the function it will perform in the grid [3], [7], [11].

Which could be for improving the power quality, transmission and distribution grid support load shifting and bulk power management. Fig. 5 shows the comparison.

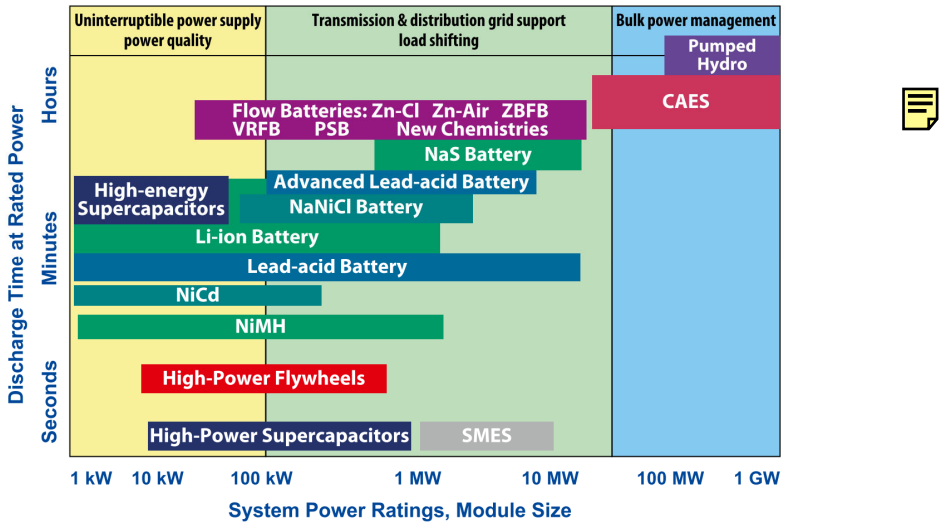


Fig. 5 Energy storage devices ordered based on their power rating and discharging times, and their possible application in the grid [3].

Supercapacitors (SCs) are energy storage devices with the highest power density relative to Li-ion batteries, flywheels, fuel cells and superconducting magnetic energy storage systems [8], [10]. Therefore, they are very suitable for maintain the power quality in the grid for a period of time in the second's range.

Although SC technology is still developing, the basic principle of storing energy in a SC is through physically separating positive and negative charges as in a normal capacitor. The main difference between a capacitor relies in the porous electrodes that hold the charges, and between those porous electrodes there is an insulator placed in the middle of both positive and negative plates [10]. Fig. 6 shows the composition of a single SC cell.

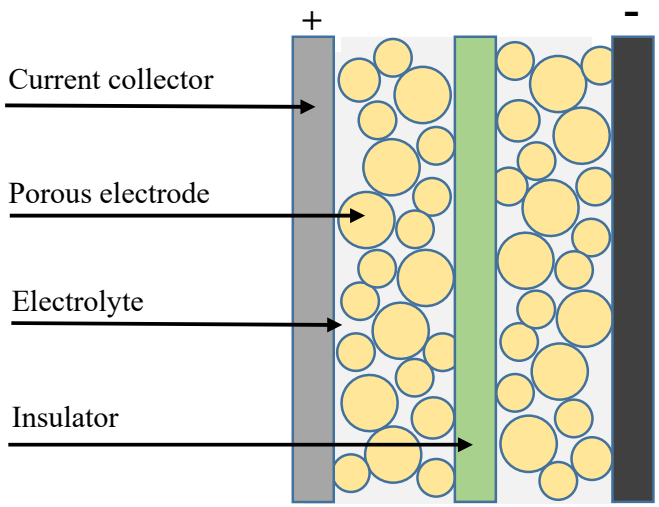


Fig. 6 SC single cell composition.

This high-power density comes with a cost, namely that SCs are usually low voltage devices, around 2.5V to 3.0V maximum [12]. This problem can be overcome by using series connections with passive or active balancing systems, the latter being more efficient [13], [14]. However, in terms of design, this added circuitry creates a more complex and expensive ESS that is also susceptible to failure because of the many parts involved in the system [15], [16].

Moreover, as they behave as a normal capacitor, their Energy capacity *E* is defined as:

$$E = \frac{1}{2} C V_{MAX}^2, \qquad (1)$$

therefore, if we want to use around 75% of its energy capacity the voltage range would have to vary from [$V_{MAX}/2$, V_{MAX}]. This creates another limitation in which the power converter has to operate efficiently in the entire voltage range.

Typical applications of SC-based ESSs are related to fast energy injection [17]. For example, in isolated microgrids with a high penetration of renewables [18], SCs maintain the power balance between consumption and generation, because inertia mechanisms are limited.

A review of multiple SC-based ESSs for microgrid applications is presented in [19]. In 2018, 29 out of the 985 electrochemical projects are based on SCs, and the total power of these projects is 34.273 MW. The reviewed ESSs provide 5 top services such as voltage support, transportation services, electric energy time shift, frequency regulation and renewables capacity firming. Other cases are transmission support, ramping and load following.

Supercapacitors can provide an alternative to spinning reserve for frequency regulation services [20]. Hence, SC-based ESSs are a suitable offer for grid ancillary services since they have the required high power energy storage for short periods [21], [22].

Other authors have studied incorporating SCs in low-voltage MMC, for example, for railway traction systems in which each SC is integrated in every Submodule (SM), but only studied analytically [23]. Another SC Low-voltage MMC application was also studied in STATCOMs by incorporating the ESS into the MMC, however it was only possible by adding an additional DC/DC converter [24]. The same occurs for a power traction converter, adding SCs as temporary energy storage with an additional DC/DC converter [25].

1.3. ESS grid synchronization

Due the nature that the majority of energy storage devices only store energy in the form of DC, it is not possible to directly interconnect them to the AC grid. Therefore, several subsystems have to be implemented in the ESS to accomplish the so-called grid synchronization.

This requires a DC/AC inverter and complex controller circuitry that ~~it~~ is supervising constantly the power flow from DC to AC and the voltage in both AC and DC sides. If 4-quadrant operation is required, then the circuitry has to be able to adjust active and reactive power as well.

For any type of ESS or inverter-based system there are two forms of operating the DC/AC inverter: grid-following or grid-forming converter control [26]–[29]. Being the grid-following control the most used in PV and wind inverters in todays' applications. The grid-forming control is under development and only a description of how it should operate or behave was introduced in [30]. The description presented of both controls is extracted from [26]:

In a grid-following inverter, the current injected by the inverter to the grid is controlled with a specific phase shift from the grid voltage at the Point of Common Coupling (PCC). Thus, the fundamental frequency phasor of the grid voltage is needed at any time for the precise calculation of the inverter's reference current, whose amplitude and angle with respect to the grid voltage phasor are properly modified by the outer controllers to inject the required amount of active and reactive power or control the RMS voltage.

In a grid-forming inverter, the magnitude and angle of the voltage at the PCC are controlled by the inverter. Hence, the fundamental frequency phasor of the grid voltage at the point of connection is not strictly necessary to be known. Based on the type of network to which the inverter is connected, an isolated system or a slack bus, it is possible to adapt the injected instantaneous active and reactive power using additional outer controller loops, to provide voltage and frequency support. In an isolated system, a grid-forming inverter could behave itself like a slack-bus. When connected with other power sources, through an inductive line, the grid-forming inverter is controlling the active power by adjusting the angle. The voltage magnitude is independent of the active power control.

Since ESSs already have the required energy buffer for successfully operate in the grid-forming control, they can also be used as to provide frequency support and black start services.

Many authors have proposed grid-following algorithms that have proven to allow the rapid expansion of renewables integration to the grid [31]–[33]. However, if we want to continue the further penetration of renewables into the grid, authors have started to study the impact of the many inverters with rigid control schemes based in the grid-following. Alerting the problems that could arise under this phenomena [30], [34].

1.4. The basic elements of ESSs

An ESS needs to keep the energy storage devices or cells balanced, protect them from overvoltage and create the output voltage using bidirectional DC/DC to provide and stable voltage for the DC/AC inverter. A basic ESS is composed of a balancing system (if the cells cannot exceed its capacity/voltage rating), the energy storage devices or cells,

a bidirectional DC/DC converter, a DC link capacitor, and a bidirectional DC/AC converter, as Fig. 7 shows [17], [35].

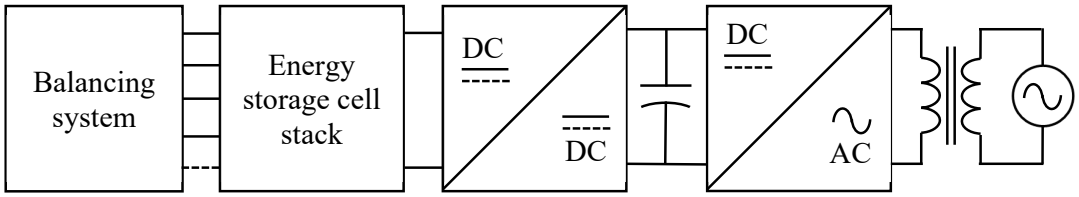


Fig. 7 ESS basic block diagram.

The balancing system must be selected depending on the technology used for storing the energy. For any lithium-based battery it is important to always keep the battery cells balanced, and if there is a necessity to correctly measure the State of Charge (SOC), then instead of using only a balancing system it is necessary to include a Battery Management System (BMS). Which can supervise the cells voltages, currents and the temperature also for an extra layer of protection, allowing the BMS to protect the cells from overcharge, over-discharge, over-current or short-circuit [36].

The same concept of using a BMS applies for any battery technology that has to keep voltage and current levels within certain range. For example, this is also true for lead-acid batteries, although they can withstand or tolerate the overcharge condition in comparison to lithium batteries, they will start to degrade faster if the cells are not properly matched.

If other type of technology is used and there is a necessity to supervise various parameters of the device, then a more general Energy Management System (EMS) has to be implemented. For example, for flywheels it is necessary to measure the rotor speed and the moment of inertia. In CAES the parameters are pressure, volume, temperature,

and discharge profile. Therefore, the EMS will behave differently depending on the energy storage technology implemented [37].

For SCs, the simplest approach is to guarantee that the cell stack is voltage balanced, resulting in a balancing system that only needs to measure the voltage of each cell and then balancing the cells accordingly. If a passive system is used, the most used method is to slowly discharge the overcharged SC cell. However, the passive method will waste the excess of energy in the form of heat, which increase the temperature of the stack if there is no proper heat dissipation. Therefore, although the active method is more complex, it is the most suitable since the excess of energy from one overcharged SC cell is transferred to another one, with efficiencies ranging from 70 to 90%. If there is a necessity to supervise the SOC of the SC stack and other parameters, then a Supercapacitor Management System (SMS) has to be implemented. Many authors have proposed different methods to analyze the SOC of the SCs, the main goal is to fit all the physically measured data into a model to accurately determine the SOC [38].

Mainly, SC voltage changes linearly with the state of charge, so a DC/DC converter with a wide input voltage range and a constant DC output voltage is commonly needed [39]. A DC link connects the DC/DC converter to a traditional DC/AC converter, which creates an AC signal. In addition, as galvanic isolation is important when the ESSs are connected to the grid to avoid stray currents or DC currents. A bulky 50Hz transformer must be used if none of the other stages has isolation, which increases the converter's size. Each of these circuits or stages requires a careful design process to accomplish the power budget.

1.5. Objective of the research and methodology

In a traditional SC based ESS, four stages are needed: the energy storage devices, the balancing system and the DC/DC and DC/AC converters that connect the storage devices to the grid. The main contribution of the proposal is an SC-based ESS which reduces the number of stages by adopting the Modular Multilevel Converter (MMC). Thus, it is possible to create an ESS with increased efficiency since less losses from the stages are present.

Instead of the traditional approach, the MMC can be used, which is based on a high voltage DC source and a series of submodules (SMs). In this system, the DC/DC and DC/AC conversions are performed in the SMs, which consist of DC/DC converters. These MMC topologies have been used in HVDC transmission [40], [41]. One of the main advantages of MMCs is the simplicity in scaling up the voltage of the system by adding more SMs to the MMC [42].

The relevant aspect of this work is to integrate a single or a few SC in each of the SMs, and therefore, no high voltage DC source is needed. In addition, each SM works in a voltage range of a few volts, which allows the use of low-voltage switches, with low conduction losses [23] and makes possible a low total harmonic distortion (THD) of the AC output voltage and current.

The research addresses the design methodology of the MMC, the selection of a proper DC/DC bidirectional topology for each SM, the internal SM voltage/energy balancing problem, the grid synchronization, and the ability to inject or absorb active and reactive power from the grid efficiently.

The objective is to demonstrate with a fully operational small-scale prototype the ability to perform the self-balancing process and the DC/DC and DC/AC conversions in a single stage by adopting the MMC topology for Low-Voltage energy sources as the SCs. Hence, the novelty of this work resides in the selection, design of the power converters and the proposed techniques to use them as balancers, DC/DC, and DC/AC converters simultaneously. Saving size, reducing cost and increasing the flexibility or modularity of ESSs.

Great efforts were done in order to experimentally validate the proposed strategy and ESS. Results are a real working prototype with an outstanding efficiency using standard silicon semiconductor transistors.

Simulations were done using Matlab Simulink and LTSpice or HSpice, Python and Numba library for highly intensive CPU simulations. For the experimental part multiple PCBs were designed and fabricated at the Skoltech Power Electronics lab, and the testing of the prototypes required high-current measurement probes.

2. Literature Review

Most ESS have an interface between the energy storage device and the grid or microgrid, which is the DC/DC converter. Depending on how the energy storage device operates the DC/DC converter has to be suitable for extracting the most energy of it, and with great efficiency in both directions. Therefore, the DC/DC converter must be designed to operate in the range of voltages and power levels required by the energy storage device. Normally, for stationary applications in the grid or microgrid there is no constrain in the volume of the converter, but if the ESS is implemented for mobile or

vehicle applications, then this also has to be taken into account, as well as the total heat dissipation of the ESS.

This section is devoted to give an overview of the state-of-art of the DC/DC converters and DC/AC inverters developed for ESSs applications. Since the proposed ESS uses SCs as energy storage device then the constrains for the DC/DC converter are mainly that they need to be wide input voltage range, high power handling, bidirectional power flow and high efficiency.

Many authors have proposed different techniques to accomplish the wide input voltage range, one of the basic principles is to use various cascaded stages to obtain a stable voltage output. The first stage elevates the voltage to a certain level using a boost converter topology, and then, the subsequent stages are in charge of regulating the voltage to a suitable level for the DC/AC inverter.

In this section, several types of topologies for DC/DC converters and DC/AC inverters will be covered, namely, high-gain DC/DC converters, bidirectional multi-level converters, bidirectional inverters including multi-level converters, MMC and their basic SMs topologies, and finally, a comparative of actual ESSs, their efficiencies, costs, Total Harmonic Distortion (THD) and volume.

2.1. High-gain DC/DC converters

High-gain DC/DC converters are of special importance if the energy storage device operates in a low-voltage level. As discussed in the previous section, it is possible to place the energy storage devices in series to increase the voltage, but if they cannot surpass a certain voltage level or rating, then it is mandatory to introduce a balancing

system. However, if too many cells are placed in series, the complexity of the balancing system will increase too. Therefore, this is the reason of implementing a high-gain DC/DC converter which can boost the voltage from the energy storage stack to desired levels to use with the DC/AC inverter. For example, off-grid inverters boost the 48V input voltage from lithium or lead-acid batteries to 400V so the DC/AC inverter can operate at 220 or 230VAC levels.

Authors in [43] presented a high-gain bidirectional quadratic DC/DC based on coupled inductor with current ripple reduction capability. By using the coupled inductor, the converter can operate in b power flow modes with a reduced ripple current at both input and output ports. The voltage gain for the boost-mode is as high as two cascaded boost converters, and the same applies for the buck-mode, hence a high-gain is achieved. The authors analyzed in detail the operation in continuous conduction mode, discontinuous conduction mode as well as the boundary conditions. The prototype of 250W with a low side voltage of 27V was able to boost it to 110V in the high side output. The efficiency achieved by the prototype stayed above 90% for both boost-mode and buck-mode, in a wide range of power variation.

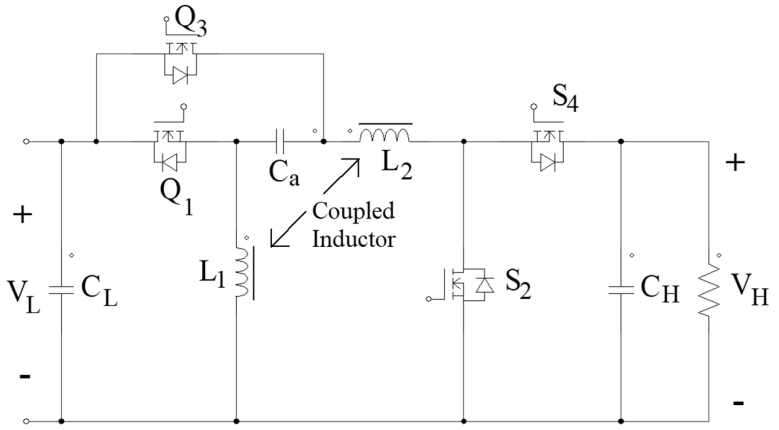


Fig. 8 High-gain bidirectional quadratic DC–DC converter based on coupled inductor.

In [44], the authors have proposed a wide input range DC/DC converter suitable for fuel cells, this circuit was also tested with commercial SC modules inserted before T_1, at the input side. The proposed converter was able to take an input voltage of 42-60V and provide a stable output voltage of 400V with a maximum power of 5kW. A two stages approach was used, the first stage is a three-level boost converter cascaded with the second stage, a current-fed two-inductor boost converter topology, which has a higher voltage gain and provides galvanic isolation from the input source. The first stage was designed to boost the voltage from the wide input of 42-60V to 80V, so the cascaded stage works always in its optimal voltage input in terms of efficiency. A total efficiency of 92% was achieved with the converter. Fig. 9 shows the proposed DC/DC converter.

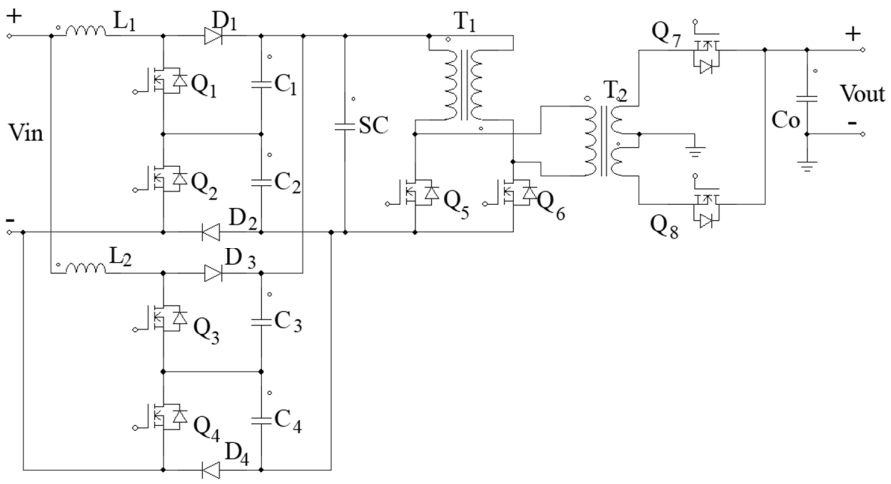


Fig. 9 Wide input range DC/DC converter composed of two cascaded stages.

In [45], the authors proposed a new converter by combining two half-bridges and the resulting converter along with the proposed PWM plus phase-shift control is able to operate with high-gain and soft-switching characteristics. Fig. 10 shows the proposed converter, C_a is used to couple the two half-bridges, and V_H is the sum of the output voltage of the first bridge plus the output voltage of the second bridge. The built 3kW prototype was able to convert from a high side voltage of 450V down to 86V, achieving efficiencies values greater than 96% in both power flows. Since the converter can achieve Zero Voltage Switching (ZVS) at all load and voltage conditions and in both power flows, the high efficiency is maintained for wide operating power. However, the main drawback of this converter is that V_L and V_H are not isolated.

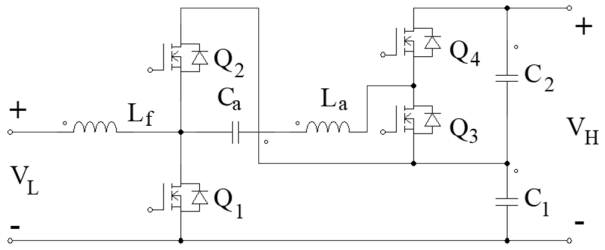


Fig. 10 High-gain soft-switching bidirectional DC/DC converter composed of two half-bridges.

In [46], a ZVS Bidirectional DC/DC converter with phase-shift plus PWM control scheme is presented. The novelty relies in solving the drawbacks of the current-voltage-fed bidirectional DC/DC converter, which are high voltage spikes and high circulating conduction losses. This was accomplished by adding an active clamp branch (C_c, S_a and S_b), and the phase-shift plus PWM control technique, therefore all the switches can achieve ZVS in a wide range of load variation and input and output voltages variations too. The 1.5kW prototype was able to achieve a voltage conversion with an input voltage varying from 22 to 32 V and obtaining a regulated voltage of 270V with efficiencies up to 90%. Additionally, this converter provides isolation due the High Frequency (HF) transformer T_1. Fig. 11 shows the proposed converter schematic.

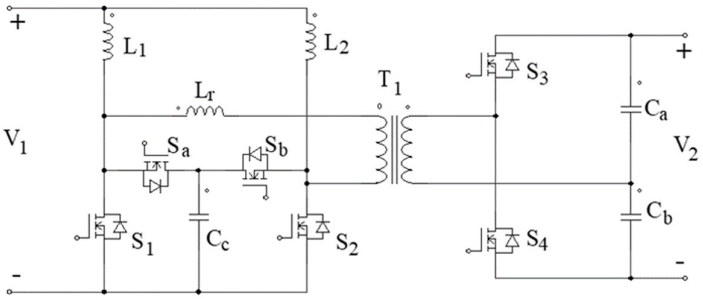


Fig. 11 ZVS bidirectional DC/DC converter with phase-shift plus PWM control scheme.

In [47], a high-gain dual-input converter is presented, which allows to connect different types of energy storage devices to create a hybrid ESS. The converter is totally bidirectional, therefore is possible to extract/storage energy with a specific energy storage device, hence a full-active configuration is achieved. With only two control signals is possible to select from which voltage source or energy storage device extract the energy or store it. Also, few components are needed, an because it does not use HF transformers there are no voltage spikes or recirculating currents. The authors proposed to use a Li-ion battery for bulk energy storage and SCs for delivering power. The converter can achieve a high gain at its output port with a quadratic expression $V_0 = V_{SC}/(1 - D_2)^2$. The built prototype was able to achieve 94% at 200W transferring power from the second input (V_{SC}) to the output. Fig. 12 shows the proposed converter schematic.

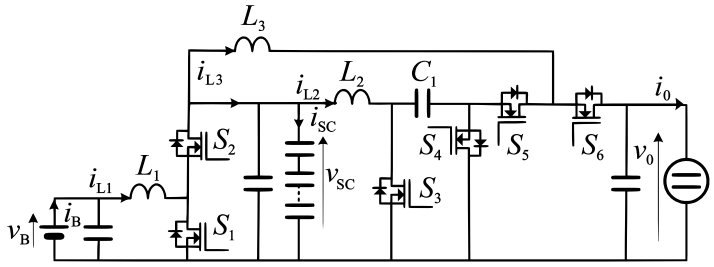


Fig. 12 High-gain dual-input DC/DC converter.

In [48], the authors proposed a full-bridge with an active clamp and the controller is able to achieve ZVS in a wide input voltage range. Although initially proposed in [49], the authors made a complete analysis of the boost-mode operation of the converter. The results were validated with a prototype which was able to boost the voltage from a varying input voltage of 22-41V to 350V at the output. In addition, they verified experimentally the ZVS operation through a wide input voltage range and power loads, achieving an efficiency of 94% with a 500W rated prototype. Fig. 13 shows the proposed converter schematic, active clamp is composed of Q_a and C_a. Although the authors only analyzed the boost-mode, in [49] the buck-mode is also analyzed, therefore the converter can be bidirectional and suitable for ESSs.

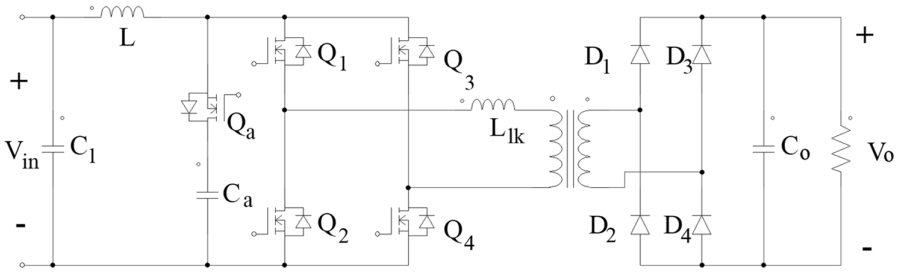


Fig. 13 Extended range ZVS active-clamped current-fed full-bridge isolated DC/DC converter.

As seen from the literature review, the techniques that allow the implementation of high-gain converters with great efficiency are the techniques of ZVS intervals and HF transformers to increase the gain even further. Moreover, the converter has to be able to operate efficiently if a wide-input range is required, or in other words, be able to regulate or work on all the possible duty cycle selection.

Based on the presented converters it is possible to categorize them and select an adequate DC/DC converter for a specific application, other considerations have to be taken into account like control complexity, cost, estimated resulting volume of the converter and so on. Traditional ESS designers select the DC/DC converter that allows them to extract the maximum energy from the energy storage device and can be paired with the DC/AC inverter too.

One limiting factor of high-gain DC/DC converters is the need of properly sizing the transistor breakdown voltage. Commercial Silicon (Si) MOSFETs are widely available from voltage ranges up to 4.7kV, however, the tradeoff would be the increased $R_{DS}(ON)$ value, which could lead to high conduction losses, this also applies for Silicon Carbide (SiC) transistors and IGBTs. Therefore, if high voltage gain ratios are needed to reach or voltages levels that are beyond the capabilities of the switches another type of topology must be selected for. Next subsection focuses on a solution for the described limitations.

2.2. Bidirectional multi-level converters

As discussed in the previous subsection, one limiting factor of any traditional DC/DC converter topology is the voltage breakdown of the transistor. One solution is two put the transistors in series and switching them exactly at the same time to share the total voltage across the transistors. However, this solution would require a complex circuitry that is able to synchronize the switching operation and might be not so practical. Therefore, a different technique is used to share the voltage across the transistors without the problems of synchronization mismatch. This can be done by using multi-level converters.

Multi-level converters are a solution for reaching higher voltages levels by using lower voltage rating switches or transistors. Although the first application of a multi-level converter were in the field of an inverter motor controller [50], the idea of synthetizing a higher voltage waveform from various voltage sources remains. Moreover, if the number of levels or stages increases it is possible to reduce the THD as each step transition will be closer to the desired output waveform. This will be better explained in the next subsection, and in this subsection a survey of bidirectional DC/DC multi-level converters is presented. Hence, the main benefits for using this approach are the possibility of reaching higher voltages by placing a series combination of lower rating transistors, capacitors, and diodes. Thus, the efficiency can be increased as the device is not handling the total voltage as in a traditional DC/DC converter, and the switching losses can be reduced as well.

Traditionally, two types of multi-level converters started to be of great importance for DC/DC power conversion, the flying capacitor and the diode clamped converters. The conventional topology for a flying capacitor multi-level DC/DC converter is presented in Fig. 14.a and composed of only 3 levels or stages as example, the converter is able to transfer power from a low voltage power source V_{LV} to a high voltage source V_{HV}. However, the switching scheme is dependent on the number stages or levels used. In this 3-level example the switching pattern for a 50kHz multi-level converter with an input voltage of 2000VDC and an output voltage around 520VDC is presented in Fig. 14.b. Notice that the duty cycle of S_{1p} to S_{3p} is only 1/3, if more levels are added to decrease the output voltage then the duty cycle is limited to 1/*n.* Therefore, in practice not so many levels can be used. But the advantage is that the transistors are not directly connected to

the total input voltage and only a proportion of the voltage is “seen” through the transistor, in this example the drain-source voltage (VDS) for both S_{3p} and S_{2n} remains below 700VDC.

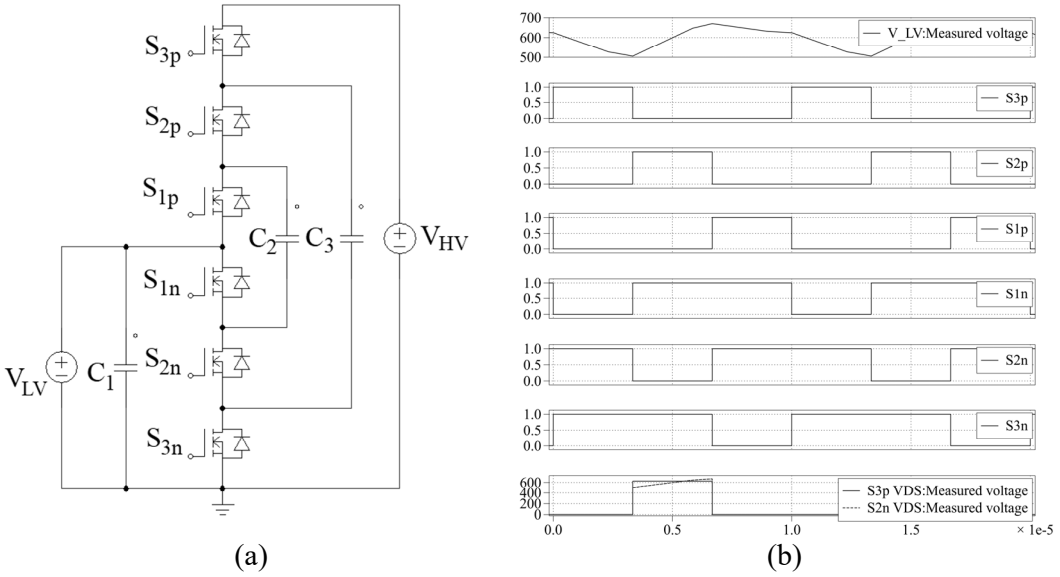


Fig. 14 Flying-capacitor multi-level DC/DC converter, 3 level example.

In [51], one of the first multi-level switched-capacitor DC/DC converter analysis is presented, if transistors are used instead of diodes bidirectional power flow can be accomplished. The authors detailed that because there are no magnetic components involved, the proposed converter can be easily implemented for monolithic integration. Fig. 15 shows the proposed converter, notice that basic block is composed of three transistors (M_n, M'_{nP} and M'_{nN}) and only one capacitor C_n. Depending on the *n* number of stages it is possible to create a converter with a $V_o = V_i .n$. Although the converter is old and uses many active elements, the analysis presented, and the proposed technique can be used for different types of switched-capacitor DC/DC converter topologies.

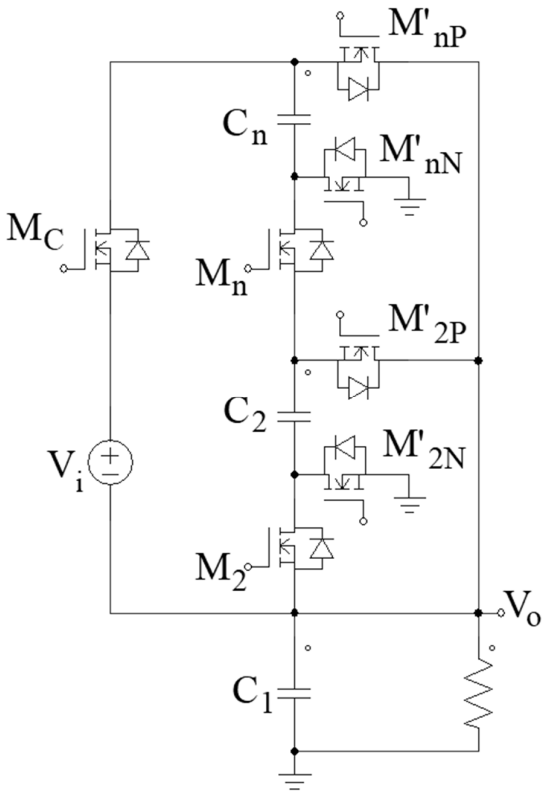


Fig. 15 An n-stage switched-capacitor DC/DC converter schematic.

In [52], the authors propose an improvement to the previous flying capacitor multi-level DC/DC converter. Interestingly, using the same topology from Fig. 15 and only changing the switching states they were able to achieve better power conversion ratio and less voltage ripple. They also validated the proposed converter for bidirectional operation. The feasibility of the converter was verified through simulations and with a prototype of 6-stages. The prototype was able to transfer power from V_i at 80V to V_o at 12V, it was able to achieve a maximum power conversion of 120W with an efficiency around 93%. However, the authors mention that the efficiency can be increased by properly selecting the transistors with a good value of $R_{DS}(ON)$.

In [53], a bidirectional multi-level DC/DC converter is presented, the converter uses no magnetic components and is able to change the voltage output almost continuously. Due the fact that there are no magnetic components, it is possible for the converter to work under higher temperature conditions. Although in reality it would be impossible to switch a capacitor due the high transient currents that can be reached, the authors take advantage of the parasitic inductance of the cable and the Equivalent Series Inductance (ESL) of the capacitor on the battery side to limit the current and therefore avoid an overcurrent condition in the transistors that could damage them. The article shows how the converter operates and the authors validated the proposed converter with a prototype which was able to increase the input voltage V_{DC} two times to V_{out}. The prototype achieved high efficiency values, higher than 98%, through the entire power load from 1kW to almost 11kW.

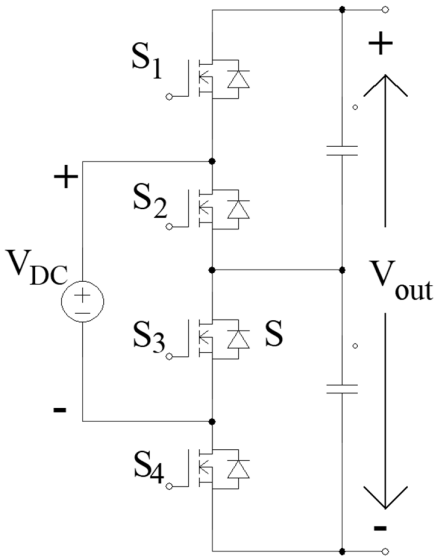


Fig. 16 Multi-level bidirectional DC/DC converter with high efficiency.

In [54] a SiC-based bidirectional multi-level high-voltage gain switched-capacitor resonant converter is presented. The converter is based in the same principle of multilevel topologies and therefore it can achieve reduced voltage stresses on the switches, high voltage gains and bidirectional conversion ability. Furthermore, the proposed converter transfers energy via the capacitors, hence the weight of the converter is reduced in comparison to inductive-based ones. The authors presented a four-level prototype which was able to reach a V_{HV} of 2kV and 500VDC at $V_{LV,}$ using SiC transistors for increased efficiency and power ratings. The prototype was able to reach up to 5kW and efficiencies higher than 97%. Since four levels were used, the V_{DS} for the transistors will not exceed 650VDC, allowing to use Si or SiC transistors in that range. Fig. 17 shows the schematic for the four-level resonant multi-level converter.

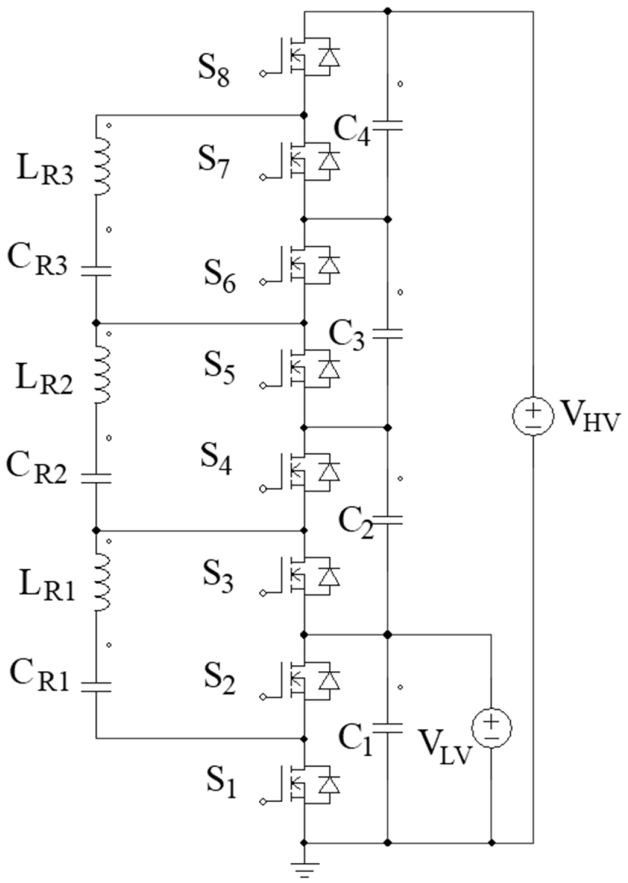


Fig. 17 SiC based high-gain bidirectional DC/DC multi-level resonant converter.

As demonstrated by the authors, multi-level converters possess many advantages for creating DC/DC converters with reduced voltage stresses on the switches and as seen from some of the proposed converters, they can create output waveforms with low distortion, which would be suitable in the next subsection discussing the multi-level converter topologies for inverters. However, one disadvantage is the increased number of gate-drive circuits that have to be interfaced relatively to each transistor. Therefore, if many levels or stages are required for reaching a specific high-voltage level, the many

gate signals can be the limiting factor to escalate the converter, or reliability can be a concern due to the many circuits involved.

2.3. Bidirectional inverters including multi-level converters

This subsection details the main aspects and topologies of bidirectional inverters. Similarly, to bidirectional switched DC/DC converters, DC/AC inverters are also able to deliver positive voltage and both negative and positive currents, but also with the possibility to deliver negative voltage with both negative and positive currents as well, Fig. 18 shows the described four-quadrant operation. Some DC/DC converters can achieve that four-quadrant operation too, but the main difference is that DC/AC inverters are designed to work with a higher switching frequency to track a fundamental AC frequency. 50 Hz or 60 Hz for interconnecting to grids, or higher variable frequencies for motor control [55].

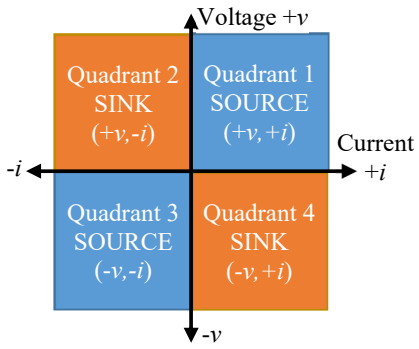


Fig. 18 Four-quadrant plot for bidirectional DC/AC inverters.

Therefore, a traditional full-bridge composed of switches or transistors can be used as the most basic DC/AC inverter if a single DC power supply is intended to invert, in which the AC load or AC output is connected in between of each switch arm. In

addition, the half-bridge topology can be used as a DC/AC inverter if positive and negative power supplies are used, with the load being connected between the transistor arm and the middle point in the power supplies.

As mentioned in the previous subsection, the first development of multi-level converters was in the field of inverters [56]. As they first were intended for industrial applications, specifically for controlling high-power motors, but now, particularly, this type of inverters can help to interconnect renewable sources to a medium-voltage grids [57]. Again, the benefit of multi-level inverters comes in the possibility to use various switches or transistors with a lower voltage rating than the desired voltage level. For low-voltage applications, using multiple stages will reduce the output filter size or the THD.

The two popular types of multi-level inverters are the diode-clamped and capacitor-clamped. As already illustrated in Fig. 14, the capacitor-clamped type can be reconnected as shown in Fig. 19 and generate a sinusoidal wave form at V_{an} connection port. C_2 will provide the neutral point if a single high voltage power supply is used (V_{HV}) [58]–[60].

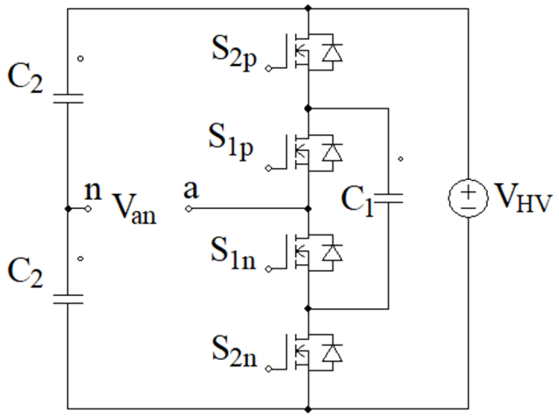


Fig. 19 Capacitor-clamped 3-level DC/AC multi-level inverter.

The diode-clamped, or also called the neutral-point clamped, DC/AC multi-level inverter is shown in Fig. 20. As mentioned in the previously subsection, this three-level inverter was the starting point for the term multi-level [50]. Authors started to introduce new control techniques and therefore the development of better topologies appeared.

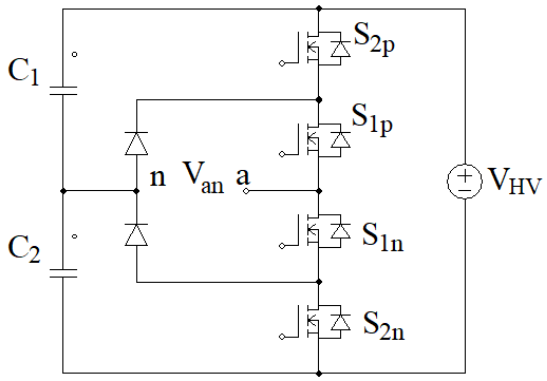


Fig. 20 Diode-clamped 3-level DC/AC multi-level inverter.

By scaling up the diode or capacitor clamped topologies it is possible to interconnect a higher voltage source to the converter, and with more levels it is also possible to generate more steps when reproducing a sinusoidal wave, hence reducing the harmonic distortion value. However, if too many levels are used, it might introduce unbalance problems and more complexity in the controller. For this reason, a generalized version of a multi-level inverter was proposed in [61], in which these unbalance problems are no longer present and also with the analysis proposed the capacitor or diode clamped versions can be derived. In Fig. 21 the P2 cell is shown as well as a 5-level example.

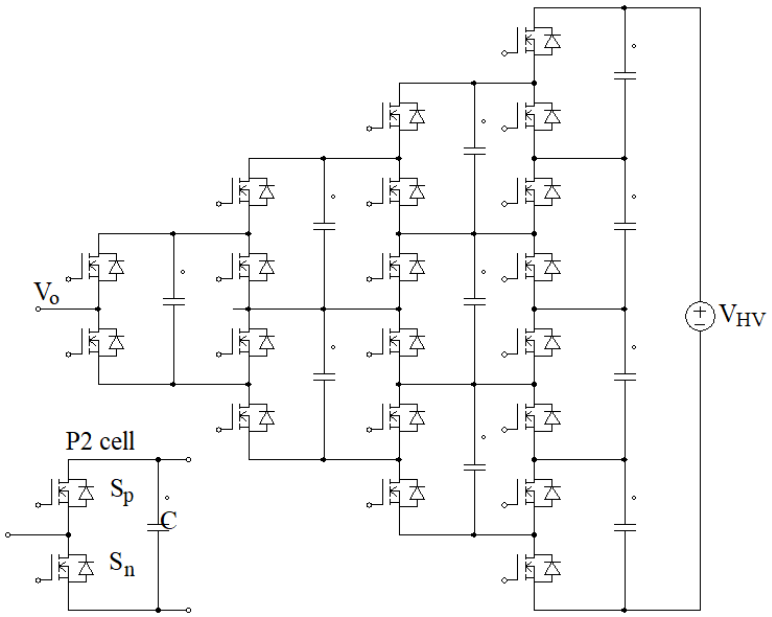


Fig. 21 Generalized multi-level DC/AC inverter with P2 cell.

Based on the proposed P2 cell other authors started to develop new topologies by modifying this basic cell, by adding new features like ZVS [62]–[64] or increased degree of control for the output waveform with different control techniques [65]–[67].

The benefits in low-voltage applications of multi-level topologies are the reduced switching losses if the number of stages is properly selected [68]. Authors addressed how to select the correct number of stages [68], [69].

As can be seen from the multi-level topologies, the main drawback is that by increasing the number of levels there is also an increase in components number. Taking for example the P2 cell, for a desired number of levels (L) would need a transistor (Q) count $Q = (L)(L\text{-}1)$. Therefore, each level increase supposes a cost increase and an efficiency decrease as more energy will be dissipated through the many transistors if they

are not properly selected. These drawbacks have been already addressed and now authors focus their attention on Modular Multilevel Converters.

2.4. MMC and their basic SMs topologies

Since the development of multilevel converters other authors started to propose new methods to arrange the levels or stages involved in the topology. Eventually, this vast research interest led to the introduction of Modular Multilevel Converters in 2001 [70]. MMC are a type of multilevel converters that consist of several Submodules (SMs) connected in series or parallel to form a multilevel voltage waveform. They have lower switching losses because they operate at lower switching frequencies and use fewer switches per SM. In addition, they have lower harmonic distortion because they produce more voltage levels with fewer SMs. Moreover, they have higher modularity, since each SM is a small subcircuit added in series. Meaning more flexibility because they can easily adjust their voltage rating by adding or removing SMs. Without the scalability issues of multi-level converters as there is no quadratic expression in the transistor count for increasing the number of SMs.

MMCs have been deeply studied for High-Voltage DC (HVDC) energy transmission applications. Even though is an expensive technology, the benefits for implementing it in large-scale projects turn them a viable solution in contrast with traditional AC transmission lines, as they provide a more robust and efficient way to transfer energy along long distances [41], [71]–[73]. In comparison to other types of topologies used for HVDC [56], [74], MMCs can be escalated as the requirements for HVDC lines increases by simply adding more SMs as shown in Fig. 25.a. MMC low-

voltage applications started to develop and this entire subsection is devoted to compare different MMC-based ESSs.

The most important part of MMCs is the SM. The chosen topology for each of the SMs will impact in the possible voltage step that each SM can produce and hence in the total required amount of SMs to tolerate the required voltage rating. Furthermore, if more voltage steps are allowed, THD could be improved, useful for low-voltage applications too. However, the complexity for operating each SM will increase if more switches are added. The very basic SM topology uses only two switches, arranged in a half-bridge design, it allows to connect or disconnect the embedded capacitor in the SM as shown in Fig. 25.b. If the SM needs to operate with positive and negative voltages, another pair of switches can be added to create a full-bridge design, thus allowing four-quadrant operation at cost of doubling the number of switches. Fig. 25.c shows the Full-bridge SM.

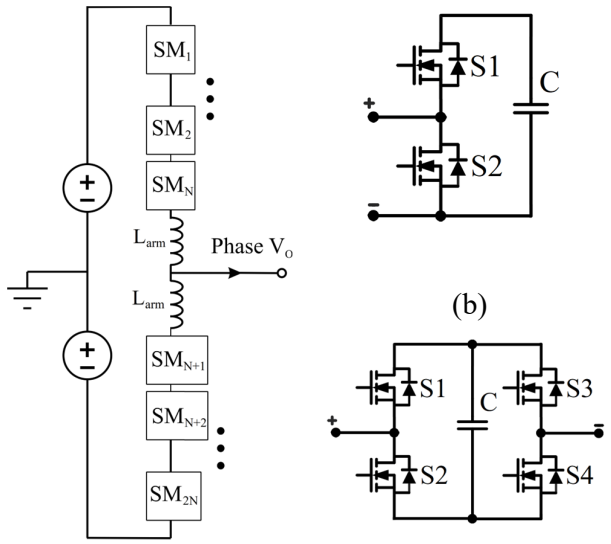


Fig. 22 Modular Multilevel Converter, (a) basic block diagram, (b) half-bridge SM and, (c) full-bridge SM.

From Fig. 22.we can see that for generating a single-phase voltage (V_O) two arms are needed and for each arm there is an inductor L_{arm} placed in series with the SMs to avoid inrush currents when connecting the SM capacitor, hence each arm behaves as a controllable voltage source. Therefore, each SM will affect the waveform of V_O. Taking for example the half-bridge SM from Fig. 22.b, if switch S2 is closed or ON and S1 is OFF the C capacitor is bypassed, and if S1 switch is ON and S2 is OFF, the C capacitor is connected to the terminals of the SM. For this reason, each arm voltage is determined by the SMs, for the upper arm the positive and for the lower arm the negative, which are defined as:

$$\begin{aligned} v_{positive} &= \sum_{k=1}^{N} V_{SM_K} \\ v_{negative} &= \sum_{k=N+1}^{2N} V_{SM_K} \end{aligned}, \tag{2}$$

hence two reference signals are needed, one for each arm:

$$v_{REF_{upper}} = \begin{cases} \dfrac{V_O \sin(\varphi)}{n_{SM}}, if\ 0 < \varphi < \pi \\ 0, if\ \pi < \varphi < 2\pi \end{cases}, \tag{3}$$

$$v_{REF_{lower}} = \begin{cases} 0\ , if\ 0 < \varphi < \pi \\ \dfrac{V_O\ sin(\varphi - \pi)}{n_{SM}}, if\ \pi < \varphi < 2\pi \end{cases}. \tag{4}$$

However, as already discussed in the previous subsection, if many SMs are added or if there is a mismatch in the capacitor's voltage in the SMs this could lead to an increase in power losses or the inability to operate at all. For this reason many authors proposed

different control techniques to keep stable energy levels among all the capacitors in each arm and also balancing both arms properly [75]–[78].

As the MMC technology matures, authors started to research the possibility of using MMCs as interface between energy storage devices and the grid, this allows creating an ESS capable of achieving all the advantages that MMC possess, and mainly for straightforwardly allowing the implementation of ESSs at low-voltage or medium-voltage levels. Several authors have presented multiple topologies based on MMC to incorporate SCs as the main energy device, due to the increased cycle life in comparison to batteries and because SCs can fulfill the high-power requirement, useful for grid operators to sustain the power quality of the grid as shown in Fig. 5. Another application is in power traction converters and by adding supercapacitors, kinetic energy can be recovered from the motor within the same converter [25]. For these reasons this literature review will mainly cover SCs as the main energy device, and only MMC topologies that are intended for incorporating an energy storage device. A review and comparison of newer advanced SM cells can be found in [77].

SCs can be added by integrating them into the SMs as presented in [79], [80]. Most authors have chosen for modifying the basic SM cell variant, the half-bridge structure, to incorporate the SC as energy storage device (Fig. 23.a and Fig. 23.b). From Fig. 23.a, it can be seen that the half-bridge SM has a lower transistor count. However, as the SM works as a two-level block: the output is either the capacitor voltage or zero. Due to that, if the SM voltage is high, many SCs (or capacitors) must be introduced in series. However, this would create a more complex SM as it will require a balancing system for each of them. Hence this topology is limited in terms of the maximum voltage in each

SM. However, if the quantity of SMs is high, the Total Harmonic Distortion (THD) will remain low. Fig. 23.b presents a solution for the aforementioned limitations of the proposed cell shown in Fig. 23.a, by including a boost DC/DC converter as an interface to the SC, thus it is possible to achieve higher voltage levels in each SM as there is no limitation from the SC voltage rating. The drawback is the increased number count of transistors and their controller; although intended for motor operation, the ESS control scheme is described in [25]. In addition, the efficiency of the DC/DC boost converter could impact on the overall efficiency of the ESS as this converter is a hard-switch topology.

If efficiency is a critical factor, an SM with soft-switching capabilities can be used, at the cost of involving a more complex controller [42]. This can be done by redefining the SM cell to take advantage from soft-switching techniques to increase the effective power absorbed or injected from the SC. This more complex SM is shown in Fig. 23.c. The SM cell benefits from the soft-switching techniques and a high efficiency could be achieved easily in contrast with the previous SM cells from Fig. 23.a and Fig. 23.b. Furthermore, instead of increasing the transistor count, this topology uses diodes and a transformer to achieve a high voltage conversion ratio, thus is possible to use a single SC per SM. The major drawback is the complexity of the controller for each SM.

Finally, other authors created a hybrid ESS by incorporating the SCs at DC-link level by rearranging the complete MMC topology and interconnecting the SCs through DC/DC converters [81]. Instead of modifying the SM cell, the energy storage device is connected at DC-link level as shown in Fig. 23.d. Here, the controller needed to operate each of the DC/DC converters is simpler in comparison to all the previously described

SM cells as only a single reference is needed and thus, a single PI controller could achieve the voltage regulation of the DC-link level. The drawback is the increased count of elements needed to achieve the same operation as the other compared topologies. Also, as originally presented in [81], the SM cell can incorporate a different type of energy storage device like a battery, and thus a hybrid ESS could be created.

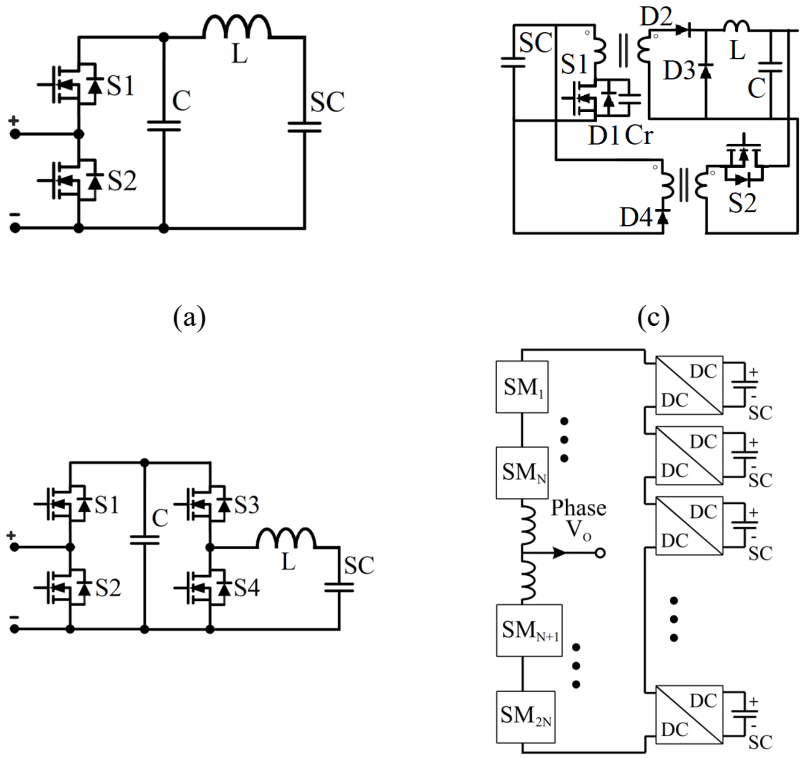


Fig. 23 (a) Half-bridge with SC connected through an inductor, (b) Half-bridge with integrated DC/DC boost converter, (c) Soft-switching SM cell and (d) Alternative MMC topology to include SCs.

2.5. Comparative of MMC-based ESSs (efficiencies, costs, THD and volume)

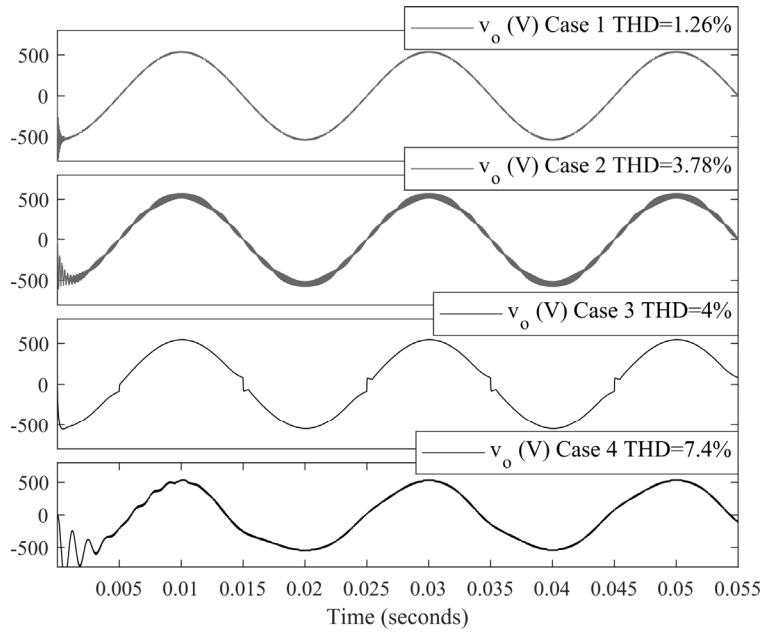
Based on the MMC-based ESSs presented in the previous subsection, a comparative study was presented in [82]. This study recovers quantitative information from each ESS, such as THD, efficiency, SMs needed, transistor count, diode count, inductors, controller complexity and costs. To make a fair comparison, the only energy storage device used was only SCs. **Table 1** shows the components used for extracting with numerical simulations the THD and efficiencies for each MMC-based ESS shown in Fig. 23. To refer to each one of the MMC-Based ESS a Case number is used further on.

Table 1. Simulation components for MMC-based ESSs [82].

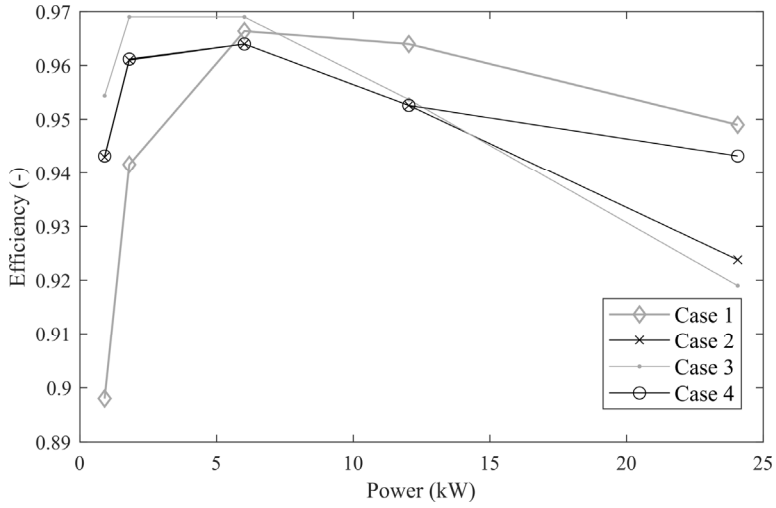
Component	Fig. 23.a [79], [80] – Case 1	Fig. 23.b [25] – Case 2	Fig. 23.c [42] – Case 3	Fig. 23.d [81] – Case 4
L_{arm}	1.2mH	1.2mH	2.4mH	1.2mH
C	100uF	240uF	1000uF	200uF
L	1uH	10uH	2.4uH	N/A|
SC	137F	166F	137F	137F
SC Model	XLM-62R1137A-R	XLR-48R6167-R	XLM-62R1137A-R	XLM-62R1137A-R
Cycle life	1,000,000	1,000,000	1,000,000	1,000,000
# of SMs	20	12	10	12
Voltage per SM	57V	95V	114V	95V
f_{sw}	20kHz	20kHz	35kHz	20kHz
S1 to S4 Model	IPP050N10NF2S	2xIPP075N15N3G	2xIPB107N20N3	2xIPP075N15N3G
S1 to S4 Max V_{DS}	100V	150V	200V	150V
S1 to S4 R_{DS}(ON)	5 mΩ	7.5 mΩ	10.7 mΩ	7.5 mΩ

The numerical simulations were done using PSIM software, the first test was configured to extract the THD of a sinusoidal waveform for further comparison between

the topologies. Fig. 24.a shows the resulting output voltage waveforms with the THD calculated for each case. Case 1 exhibits a better performance in terms of THD as it has an increased number of SMs, thus more voltage steps are developed and therefore better envelops the AC reference. Although Case 2 has a lower THD than Case 4 or Case 3, it can be appreciated a high frequency component due the DC/DC boost converters switching, a possible solution would be to only increase the f_{sw} of the DC/DC boost converter, but this results in a more complex controller inside each SM.



(a)



(c)

Fig. 24 MMC-based ESS comparison results for (a) Output voltage and calculated THD and (b) Efficiencies.

The second test bench addresses another important aspect in ESSs, the efficiency of the whole system. To accomplish this objective, multiple simulations were done, varying the requested output power. Due the fact that PSIM only calculates the conduction losses caused by the ON state voltage drop across the switches, to include the switching losses in the case of hard-switching events, as the ones in Case 1,2 and 4, those power losses were calculated considering the currents and voltages in the switches at the commutation instant in a spreadsheet and subtracted from the obtained values of the simulations. The results are shown in Fig. 24.b.

Finally, a comparison table was built using the extracted parameters from the MMC-based ESSs, **Table 2** shows the results for each Case. With these results, we create a Performance Index (PI) function to aid selecting the best Case for a particular desired application. A linear cost function with weighted coefficients was used to evaluate each case:

$$PI = k_{cost}.\frac{c}{c_{NOM}} + k_{weight}.\frac{w}{w_{NOM}} + k_{vol}.\frac{v}{v_{NOM}} + k_{SM}.\frac{SM}{SM_{NOM}} + k_{eff}.\frac{100\%}{eff} + k_{THD}.\frac{THD}{THD_{NOM}}, \tag{5}$$

where k_{cost}, k_{weight}, k_{vol}, k_{SM}, k_{eff}, k_{THD} are the coefficient which depend on the application where the sum of all of them is one, and c, w, v, SM, eff and THD are the cost ($/kVA), weight, volume, number of SMs, efficiency and THD of each case which are normalized with the nominal values.

Three applications were evaluated using the proposed PI function: Grid connected, vehicular or mobile and UPS or off-grid applications. **Table 3** shows the

values for all of the cases. Case 1 offers a simple circuit with low THD. This is a good solution for grid-connected applications, due to the increased number of SMs and because in this particular application it is not a penalty in the PI cost function having more SMs. Moving to vehicular applications, in which the volume, weight and total number of SMs are important, Case 3 is better suited, largely benefiting from the reduced number of SMs. If more efficiency is required, more transistors can be added in parallel, although this will further increase the cost of the system. Finally, for the UPS or off-grid application, both Case 1 and Case 3 are recommended, and as aforementioned, if high efficiency is a must, Case 3 can be improved by adding more transistors in parallel. However, if the system cost has to be further reduced, then Case 1 is the most suited.

Table 2. Comparative results and main aspects of each MMC-based ESS [82].

Case	THD	Efficiency	SMs needed	*S*	*D*	*L*	Controller complexity	Cost
1	1.26%	94.9%	High	2	0	1	Low	+
2	3.78%	92.4%	Medium	4	0	1	Medium	++
3	4%	91.9%	Low	2	3	1 and 2 Transformers	High	+++
4	7.4%	94.3%	High*	4*	0	2*	Low	++

*Considering the extra DC/DC converters at DC-link.

Table 3. Performance Index results.

Application	Case 1	Case 2	Case 3	Case 4
Grid connected	2.28	2.96	2.74	3.17
Vehicular or mobile	4.15	4.68	4.03	4.47
UPS or off-grid	2.55	2.89	2.55	2.83

However, from the analyzed MMC-based ESSs there is the drawback of involving an additional outer loop balancing controller for both Case 1 and Case 3 to balance the energy storage devices, hence this suppose extra computational cost besides the algorithm

that it is in charge from sorting out the SMs that should be connected or bypassed. In addition, for Case 1 there is the necessity of using many SMs, and if these SMs incorporate a single cell of low-voltage energy storage devices such as SCs then the large number of SMs could lead to an unviable solution for medium-voltage grid interconnections. Case 3 solves this problem by using a HF transformer to increase the voltage as desired by using a higher turn-ratio, however it still involves using a low-frequency switch to select which arm is connected to the grid, which could be difficult to implement in higher voltage levels. The next section describes the proposed MMC which can overcome these problems, and the SC balancing algorithm is embedded in each SM, hence scalability complexity is removed.

3. Proposed MMC

Instead of the traditional approach from Fig. 7, a Modular Multilevel Converter (MMC) can be used as authors proposed in the previous subsection for low-voltage ESSs. In this system, the DC/DC and DC/AC conversions are performed in the SMs, and the active balancing system can be performed with the proposed self-balancing technique embedded in each SM. As mentioned in the previous section, these MMC topologies have been used in High voltage DC transmission [40], [41]. One of the main advantages of MMCs is the simplicity in scaling up the voltage of the system by adding more SMs to the MMC [42], as Fig. 25.a shows for a traditional MMC topology. However, for low-voltage applications, the benefit of adding more SMs allows to further increase the energy storage capacity of the system or the power handling by placing more SMs in parallel.

The proposed MMC shown in Fig. 25.b is used to extract the energy from supercapacitors and to create a chain of voltage sources based on bidirectional DC/DC converters. The implemented submodule is a bidirectional full-bridge topology [48], [49], [83], [84]. This circuit was selected because of its straightforward use, ease of control, high efficiency, and galvanic isolation through an HF transformer. In the proposed ESS, the energy is not extracted from a high voltage DC source, but it is rather obtained from a single SC or a SC stack which is included in the submodule. Thus, the submodules contain the energy storage device and they are bidirectional.

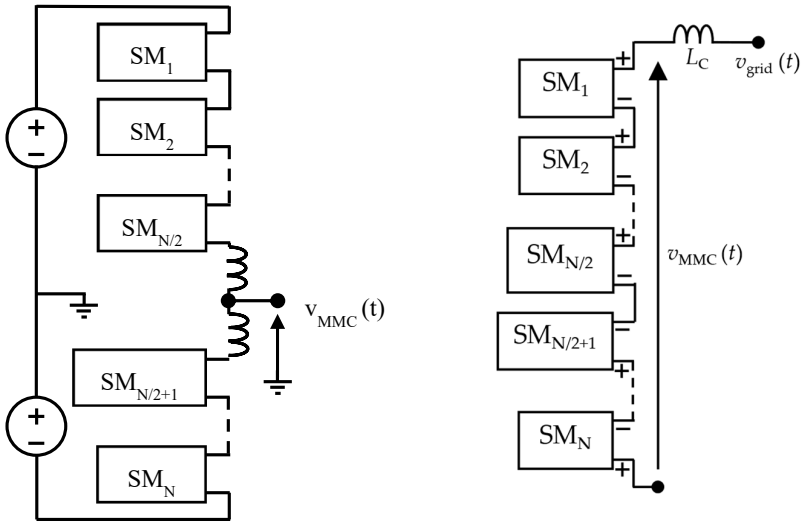


Fig. 25 Block diagram (a) of the traditional and (b) the proposed MMC topology.

Along the contributions of this research is the development of an ESS based on an MMC which can perform the functions of balancing, DC/DC and DC/AC conversions and storage in a single block, resulting in a modular converter that is easily expandable at higher voltages with an efficiency similar to traditional ESSs. In addition, this new approach based on MMC can be further improved in order to have an efficiency that is

higher than the traditional topologies using wide band semiconductors and parallel techniques.

3.1. Principles of operation

As described in the previous section, the SM is based on a well-known DC/DC converter which was selected due its characteristics of good efficiency, bidirectional, isolation and ease of control and implementation. Fig. 26 shows the schematic of the selected DC/DC converter. This is a soft-switching converter that has galvanic isolation provided by transformer T_1, uses synchronous rectification and an active clamp (C_c, Q_c) to reduce the voltage stress in the switches.

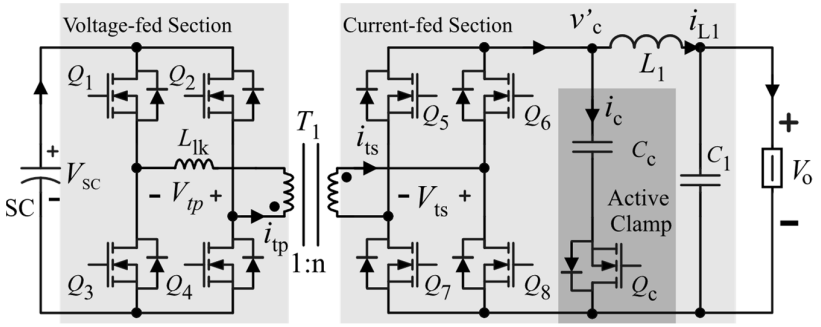


Fig. 26 Bidirectional full-bridge DC/DC converter, presented in [49].

Since the MMC has to operate in both power flow directions with high efficiency, the selected converter has to be addressed in both directions also. The converter has two modes of operation, namely, Buck-mode and Boost-mode. In the Boost-mode, power flows from the inductor L_1 endpoint to the SCs, thus the active bridge is Q_5-Q_8. In the Buck-mode power flows from the SC to L_1.

The SC is connected in the voltage-fed section and the output port is in the current-fed section. This allows wide output voltage regulation, which is necessary in order to

operate with a half-bridge rectified sinusoidal output voltage per leg. The drawback is the increase in the switches' current stress in comparison with the arrangement where the ports are interchanged, that is, the SC in the current-fed section and the output in the voltage-fed section. The circuit will be analyzed in both power flow operation modes in the following subsections.

3.1.1 Buck-mode ($V_{SC} \rightarrow V_O$)

The circuit is analyzed by taking five-time intervals (from t_1 to t_6) in one half of a switching period (T_S), as shown in Fig. 28.a. For this buck-mode, the proposed controller for the gating signals is shown in Fig. 27 and the main waveforms are presented in Fig. 28.a. Before the first-time interval (before t_1), Q_1 and Q_2 are on, and Q_3, Q_4 and Q_c are off (Fig. 28.b). This means that the voltage in the transformer's primary winding is zero (v_{tp}=0). The 2nd bridge (Q_5-Q_8) is conducting. The diodes from Q_5-Q_8 are on, and the synchronous rectifier is working, so the transformer´s secondary voltage (v_{ts}) is zero and v'_c=0, too. Therefore, no current is flowing from the primary to the secondary winding of the transformer (i_{Llk}=i_{ts}=0). The inductor current (i_{L1}) flows through the 2nd bridge and through the load. Because v_c' is zero, so i_{Cc}=0. This initial condition is the last time interval of the previous half-cycle.

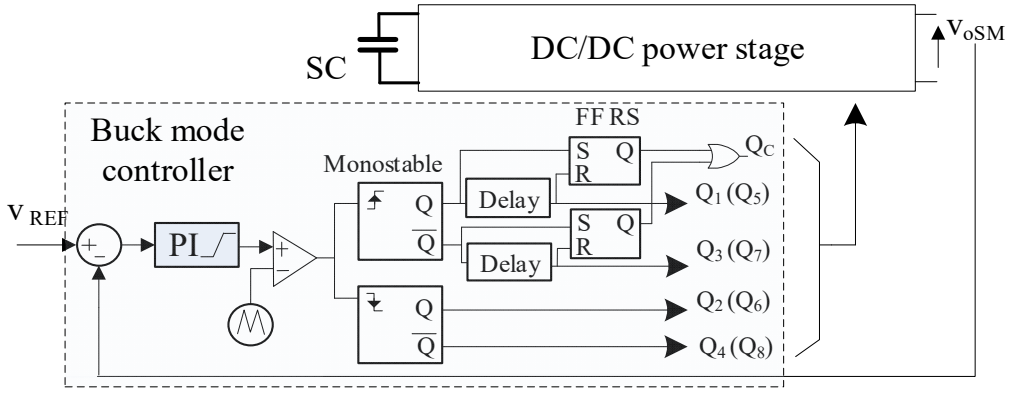
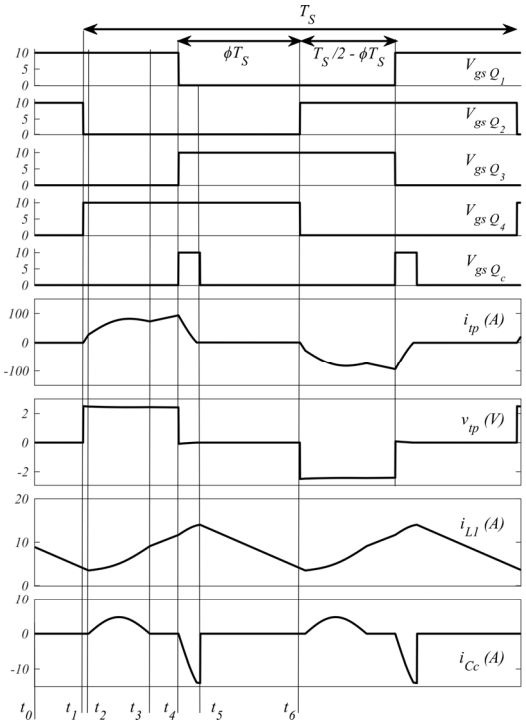
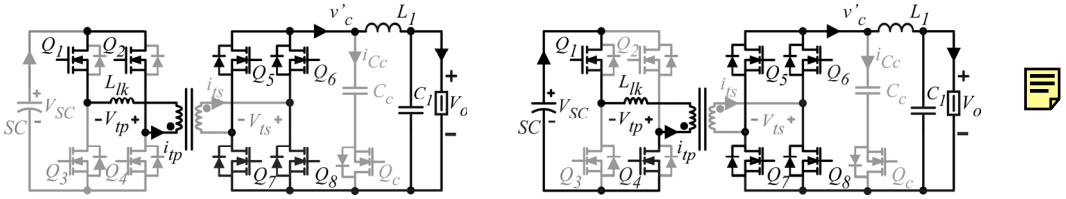


Fig. 27 Proposed SM Buck-mode controller with gating signals.



(a)



(b) (c)

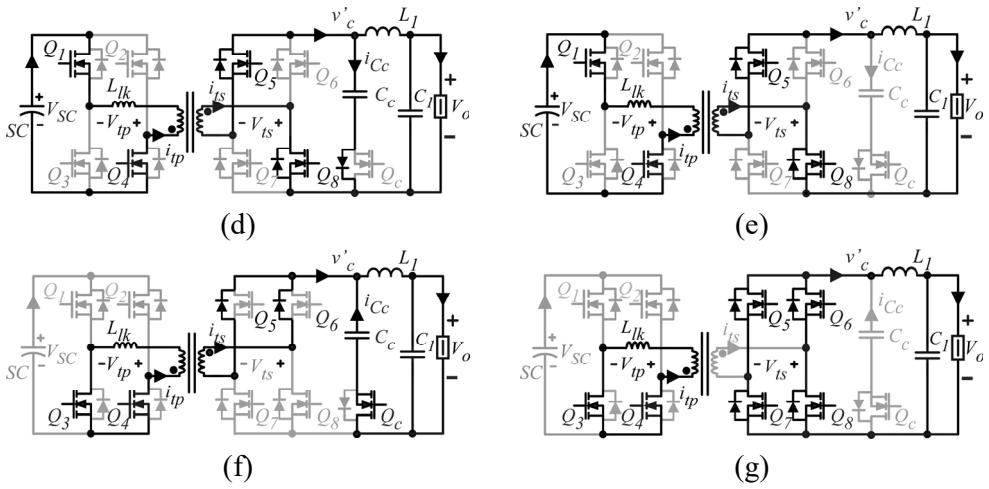


Fig. 28 Bidirectional full-bridge, (a) waveforms, (b) before 1st interval, (c) 1st interval, (d) 2nd interval, (e) 3th interval, (f) 4th interval and (g) 5th interval for the Buck-mode.

In the 1st time interval (Fig. 28.c), $[t_1, t_2]$, Q_1 and Q_4 are on, Q_2, Q_3 and Q_c are off, and $v_{Llk}=-V_{tp}=V_{SC}$. Notice that as $i_{Llk}(t_1)=0$, at zero current Q_2 turns off and Q_4 turns on; thus, both transitions occur at soft switching. $v_{ts}=0$ because the i_{L1} is still flowing through the 2nd bridge diodes from Q_5-Q_8. This interval is equivalent to the off-time in the continuous mode for a buck converter, so the inductor current follows:

$$i_{L1}(t) = i_{L1}(t_1) - \frac{V_0}{L_1}(t - t_0), \qquad (6)$$

because $v'_c=0$, and this is valid from t_1 to t_2. i_{Llk} continues increasing until the current in the secondary winding reaches i_{L1} and Q_6 and Q_7 turn off. Therefore, for the 1st time interval:

$$V_{sc} = L_{lk}\frac{di_{L_{lk}}}{dt}, \qquad (7.a)$$

and

$$i_{Lk} = i_{L_{lk}}(t_0) - \frac{V_{SC}}{L_k}(t - t_1). \qquad ((7.b)$$

The time interval ends when $i_{Llk}(t_2)=n.i_{L1}(t_2)$, where n is the turns ratio of T_1. At that moment, the 2nd time interval starts $[t_2, t_3]$ (Fig. 28.d). Q_2, Q_3 and Q_C are still off and Q_1 and Q_4 are still on (so there are no switching transitions between the 1st and 2nd intervals). Q_6 and Q_7 are already off, and v'_c starts increasing. The equations that govern the 2nd time interval are (considering $L_{mag}>>L_{lk}$):

$$V_{sc} - \frac{v'_c}{n} = L_{lk}\frac{di_{L_{lk}}}{dt} \qquad (8.a)$$

$$v'_c - V_o = L_1\frac{di_{L_1}}{dt} \qquad (8.b)$$

$$i_{Cc} = C_c\frac{dv'_c}{dt} \qquad (8.c)$$

$$\frac{i_{lk}}{n} - i_{Cc} = i_{L_1} \qquad (8.d)$$

and the solution is:

$$\frac{di_{L_{lk}}}{dt} = \left[\left(\frac{V_{sc}}{L_{lk}} - \frac{V_{sc}}{L_{lk} + \frac{L_1}{n^2}}\right) + \frac{\frac{V_o}{n}}{L_{lk} + \frac{L_1}{n^2}}\right] cos(\omega_0 t) + \frac{V_{sc} - V_o}{L_{lk}n^2 + \frac{L_1}{n}} \qquad (9.a)$$

where the resonant frequency is $\omega_0 = \left[C_c\left(\frac{n^2 L_{lk} L_1}{n^2 L_{lk}+L_1}\right)\right]^{-1}$. Considering $L_1 >> n^2 L_{lk}$, the equation can be approximated to:

$$\frac{di_{L_{lk}}}{dt} \approx \frac{V_{sc}}{L_{lk}} cos(\omega_0 t) + \frac{V_o . n}{L_1}\ cos(\omega_0 t) + \frac{V_{sc} - \frac{V_o}{n}}{\frac{L_1}{n^2}},$$

(9.b)

and integrating i_{Lk}:

$$i_{L_k} \approx \left(\frac{V_{sc}}{\omega_0 L_{lk}} + \frac{V_o . n}{\omega_0 L_1}\right)\ sin(\omega_0 t) + \frac{V_{sc} - \frac{V_o}{n}}{\frac{L_1}{n^2}} . t + I_{LMIN} . n,$$

(9.c)

where $I_{LMIN}=i_{L1}(t=t_2)$. This time interval ends when v'_c reaches $n.V_{SC}$. Using (9.c) and (8), i_{L1} is:

$$i_{L1} = I_{LMIN} + \frac{V_{sc} . n - V_O}{L_1}(t - t_2), \qquad (10)$$

which is the same equation as the one in the on-time of a buck converter. This means that the sinusoidal part of i_{Llk} flows through capacitor C_c.

In the 3rd time interval, $[t_3, t_4]$ (Fig. 28.e), Q_1 and Q_4 are on, and Q_2, Q_3 and Q_c are off (again there is no switching transition between 3rd and 4th time intervals). The circuit is transferring current from the primary to the secondary winding and works as a regular phase-shift full-bridge converter. v'_c is equal to $n.V_{SC}$, $i_{Llk}=n.i_{L1}$ and i_{L1} is still following (10).

In the 4th time interval, $[t_4, t_5]$, Q_1 and Q_2 are off, and Q_3, Q_4 are on (Fig. 28.f). In this case, a switching transition occurs when $i_{Llk}=n.i_{L1}$, and therefore there is a hard-switching process. Q_c is triggered on to release energy from C_c. This transition occurs at zero voltage, so it is a soft-switching turn-on for Q_c. During this interval two elements should be discharged: the L_{lk} inductor and the C_c capacitor. Q_3 and Q_4 make a short circuit in the primary winding, and therefore the L_{lk} inductor is discharged through the transformer and the C_c capacitor is discharged with i_{L1}. The equations that govern the process are:

$$-\frac{v'_c}{n} = L_{lk}\frac{di_{L_{lk}}}{dt} \tag{11.a}$$

$$v'_c - V_O = L_1\frac{di_{L_1}}{dt} \tag{11.b}$$

$$i_{Cc} = C_c\frac{dv'_c}{dt} \tag{11.c}$$

$$\frac{i_{lk}}{n} - i_c = i_{L_1} \tag{11.d}$$

In this case the solution is:

$$i_{L_{lk}} \approx \frac{n^2.V_{sc}}{\omega.L_1}sin(\omega_0 t) - \frac{V_O.n}{L_1}(t-t_4) + .n, \tag{12}$$

and

$$i_{L1} \approx i_{L1}(t_4) + \frac{nV_{SC} - V_O}{L_1}(t - t_4). \tag{13}$$

This behavior ends when i_{Lk}=0. However, v_c' and v_{Cc} can be different from zero. Therefore, this interval is divided into two, first, i_{Llk} goes to zero and then v_{Cc} (and v_c') also goes to zero. The first part is [t_4, t_{5a}] and the second is [t_{5a}, t_5]. Eqs. (11), (12) and (13) govern the first part. In the second part i_{Llk}=0 and only C_c and L_1 take part. The main equations are:

$$v'_c - V_o = L_1 \frac{di_{L_1}}{dt} \tag{14.a}$$

$$i_{Cc} = C_c \frac{dv'_c}{dt} \text{ and } -i_{Cc} = i_{L_1} \tag{14.b}$$

The solution for this time interval is:

$$i_{L1} = -\frac{v(t_{5a})}{\omega_0 L_1}\sin\big(\omega_0(t - t_{5a})\big) + i_{L1}(t_{5a})\cos\big(\omega_0(t - t_{5a})\big), \tag{15}$$

and this interval ends when v'$_c$ reaches zero. As [t_{5a}, t_5] is small, the solution can be approximated as $i_{L1} \approx i_{L1}(t_{5a})$, during the 4th time interval.

In the 5th time interval, $[t_5, t_6]$ (Fig. 28.g), Q_1, Q_2 are off and Q_3 and Q_4 are still on. Q_c turns off with a soft-switching process because it turns off at zero voltage and zero current. During this interval, the converter works as a buck converter in an off-state. Therefore:

$$i_{L1}(t) = i_{L1}(t_1) - \frac{V_0}{L_1}(t - t_5), \tag{16}$$

is valid from t_5 to t_6. After that, the converter starts again with the next half time of the switching period. The equations are the same, the only difference is that the short circuit of the primary winding is due to Q_1 and Q_2 during the first half-cycle and due to Q_3 and Q_4 during the second half-cycle.

The voltage conversion ratio ($M=V_O/V_{SC}$) can be obtained from the L_1 current. In a half-cycle, i_{L1} should return to the same value, which means $i_{L1}(t_1) = i_{L1}(t_6)$. Thus, M can be obtained using (6), (10), (13) and (16):

$$\frac{V_O}{V_{sc}} = n\frac{t_{5a} - t_2}{t_6 - t_{5a} + t_2 - t_1 + t_{5a} - t_2} \approx n\frac{t_5 - t_2}{\frac{T_s}{2}} \tag{17.a}$$

as $[t_{5a},t_5]$ is small then $T_S/2-\phi T_S=t_4-t_2$ and $T_{clamp}=t_5-t_4$,

$$M = \frac{V_O}{V_{sc}} \approx n\frac{T_{Clamp} + \frac{T_S}{2} - \phi T_S}{\frac{T_S}{2}} = n\left(\frac{T_{Clamp}}{\frac{T_S}{2}} + 1 - 2\phi\right). \tag{17.b}$$

The value of C_c can be obtained from [17] as:

$$C_c \geq \frac{\left(\frac{T_S}{4\pi}\right)^2}{L_{lk}.n^2} \tag{18}$$

In general, the resonant period ($2\pi/\omega_0$) should be larger than $T_S/2$, and the active duty cycle of Q_c (T_{Clamp}) is large enough to reset primary winding's current to zero.

One of the main advantages of this circuit when delivering power to the grid is that there is no need to control any duty cycle; only controlling the phase shift (ϕ) is sufficient to control the amount of energy transferred from the supercapacitor to the grid. The duty cycle for Q_1, Q_2, Q_3 and Q_4 is fixed at 50%, and this mode is called buck-mode because M follows the same equation as the buck converter, M varies linearly with the control variable: ϕ.

3.1.2 Boost-mode *($V_O \rightarrow V_{SC}$)*

In this mode, the energy is extracted from the grid, and it charges the SC. By controlling the boost voltage, it is possible to extract power from very low input voltage levels, such as found in a sinusoidal wave. In this case, the active bridge is Q_5-Q_8 and the synchronous rectifier bridge is Q_1-Q_4; the main waveforms are shown in Fig. 30. The duty cycle (D) in this mode must be larger than 0.5 for the switches of the active bridge. Q_6 and Q_7 have the same gate signals and Q_5 and Q_8 has the same as the previous but shifted 180 degrees. Fig. 29 shows the proposed controller for the SM operating in the Boost-mode.

The operation in this mode can be obtained by analyzing the waveforms and following the same procedure as in the buck-mode. Therefore, it is briefly described here, and a more detailed explanation can be found in [48]. Boost-mode consists of five-time intervals.

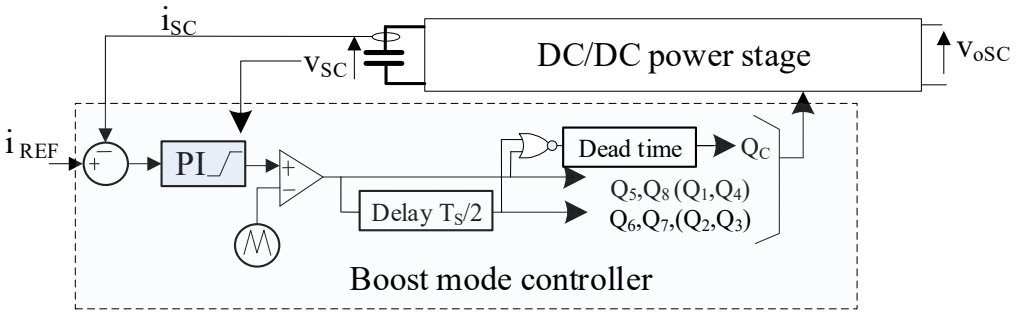


Fig. 29 Proposed SM Boost-mode controller.

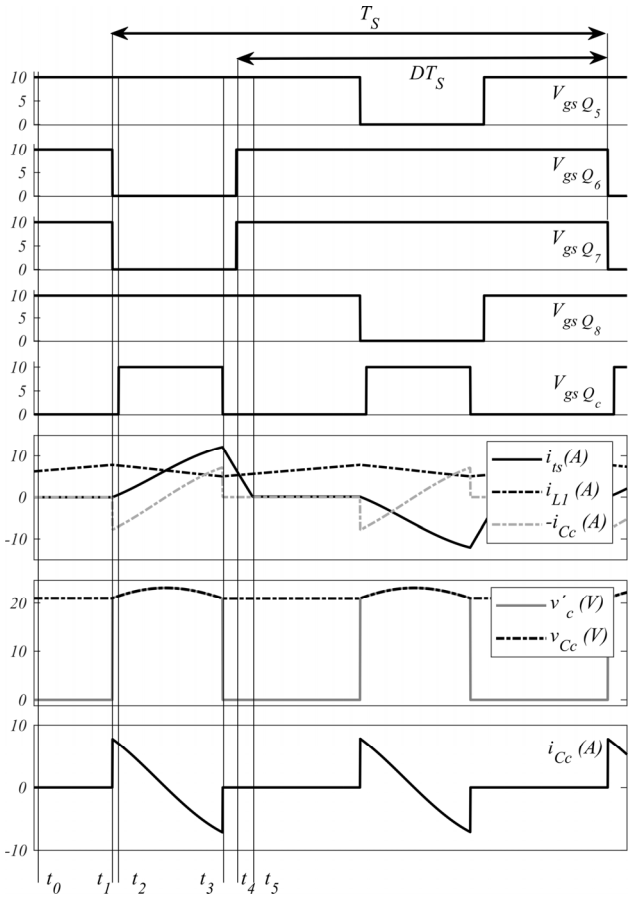


Fig. 30 Bidirectional Full-bridge Boost-mode waveforms.

In the 1st time interval, $[t_0, t_1]$, Q_5 and Q_8 are on, and Q_c is off. In this time interval, L_1 is short-circuited, as in a boost converter, i_{L1} starts to rise. During this time interval the circuit behaves like a boost converter in the on-time mode (L_1 is being charged).

In the 2nd time interval, $[t_1, t_2]$, Q_5 and Q_8 are on and Q_c, Q_6 and Q_7 are off. v'_c rises to $n.V_{SC}$, allowing Q_c to turn on at zero voltage switching (ZVS) in the next time interval. i_{L1} starts to flow from L_1 to the transformer's secondary winding. This time interval is very small, so it does not affect the profile of i_{L1}, and it is similar to the off-time mode of a boost converter (L_1 is being discharged).

In the 3rd time interval, $[t_2, t_3]$, Q_5 and Q_8 are on and Q_6 and Q_7 are off. Q_c is turned on under ZVS. The C_c current, i_{Cc}, flows and affects i_{ts}. During the first half of the interval, the current is absorbed by capacitor C_c, and during the second half it is delivered to the transformer (i_{Cc} negative). In the end, i_{L1} is less than i_{ts}. From the point of view of L_1, the converter is still working in the off-time mode of a boost converter.

In the 4th time interval, $[t_3, t_4]$, Q_c is switched off. As i_{ts} is bigger than i_{L1}, the diodes from Q_6 and Q_7 are turned on and v'_c goes to zero. When $v'_c=0$, inductor L_1 is charged again. Therefore, this time interval is an on-time interval of a boost converter.

In the 5th time interval, $[t_4, t_5]$, Q_6 and Q_7 are turned on while the diodes from Q_6 and Q_7 are still conducting, so a ZVS is achieved. The circuit keeps working in the on-time mode of a boost converter. After that, the whole process repeats but instead of Q_5 and Q_8 being the active switches, it is time for Q_6 and Q_7. This reverses the polarity of the transformer and balances the magnetic flux.

The voltage conversion ratio in this operation mode can be defined as the ratio between the period and the off-time divided by the transformer turns ratio (n). In this case, the off-time is t_3-t_1 and the period is t_5-t_0=T_S/2.

$$M = \frac{V_{SC}}{V_O} = \frac{T_S/2}{(t_3 - t_1).n} \approx \frac{T_S/2}{(1-D)T_S.n} = \frac{0.5}{(1-D).n} \tag{19}$$

The main advantage of the active clamp in this mode of operation is the elimination of almost all the voltage ringing involved in a normal full-bridge boost converter. This makes it possible to choose tight voltage devices and to reduce switching and conduction losses, thus improving efficiency. This is another reason for selecting this circuit as a submodule in the proposed MMC.

3.1.3. Small-signal analysis

The proposed MMC-based ESS has to be able to operate in AC grids or DC microgrids. Hence, a small-signal analysis of the SMs is presented in this subsection in order to validate their operation within the complete MMC in the grid. Since the proposed MMC is composed of multiple SMs interconnected in series, and each SM contains the aforementioned DC/DC converter, the small-signal analysis is done for the SM and then for the complete MMC. This analysis was presented in [85].

Let us simplify the time-interval analysis to only two main intervals. One from t_2 to t_5 where v'_c=nV_{SC}, called on-state, and the other with the rest of the intervals, where v'_c=0, called off-state. The state model for the on-state is (t_5-t_2)= ϕT_S:

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & -1/L_1 \\ 1/C_1 & -1/(RC_1) \end{bmatrix} \cdot \begin{bmatrix} i_{L1} \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 0 \end{bmatrix} . n v_{SC} . \tag{20}$$

For the off-state is (1-ϕ)Ts:

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & -1/L_1 \\ 1/C_1 & -1/(RC_1) \end{bmatrix} \cdot \begin{bmatrix} i_{L1} \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 0 \end{bmatrix} . 0. \tag{21}$$

Therefore, using the averaging approach during Ts/2, the complete model is obtained:

$$\frac{d}{dt}\begin{bmatrix} \langle i_{L1} \rangle \\ \langle v_o \rangle \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} \\ \frac{1}{C_1} & \frac{1}{RC_1} \end{bmatrix} \cdot \begin{bmatrix} \langle i_{L1} \rangle \\ \langle v_o \rangle \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \end{bmatrix} . 2\phi . \langle n . v_{SC} \rangle, \tag{22}$$

where the < > means the average in one switching period, and ϕ is shown in Fig. 28.a. In addition, for obtaining the small signal model, the variables are: $\langle x \rangle = X + \hat{x}$, where X is the average value and $\hat{x}$ is the small signal perturbation. Thus, the model in ((22) becomes:

$$\frac{d}{dt}\begin{bmatrix} I_{L1} + \hat{\imath}_{L1} \\ V_o + \hat{v}_o \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} \\ \frac{1}{C_1} & \frac{1}{RC_1} \end{bmatrix} \cdot \begin{bmatrix} I_{L1} + \hat{\imath}_{L1} \\ V_o + \hat{v}_o \end{bmatrix} + \begin{bmatrix} \frac{2}{L_1} \\ 0 \end{bmatrix} . \left(\phi + \hat{\phi}\right) . n(V_{SC} + \hat{v}_{SC}), \tag{23}$$

then, considering only the perturbations and linearizing the model the following expression can be obtained:

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} \\ \frac{1}{C_1} & \frac{1}{RC_1} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{L1} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \end{bmatrix} . n. \left(\phi . \hat{v}_{SC} + V_{SC}\hat{\phi}\right), \tag{24}$$

finally using the Laplace transformation, output as a function of the control (control-to-output) and input voltage is obtained:

$$\widehat{v_o}(s) = \frac{n. \left(\phi . \hat{v}_{SC} + V_{SC}\hat{\phi}\right)}{s^2 L_1 C_1 + s\frac{L_1}{R} + 1} = \frac{n. \left(\phi . \hat{v}_{SC} + V_{SC}\hat{\phi}\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q\omega_0} + 1}. \tag{25}$$

Thus, based on the control-to-output transfer function, a controller must be selected in order to provide in the output a DC signal plus an AC 50Hz signal. Therefore, a bandwidth of at least 500Hz is needed for the SM in order to be considered as an ideal transfer function by a high-level controller, in this case the MMC main controller. A voltage mode controller was selected due to its simplicity, but a current mode controller can be utilized as well. For increasing the bandwidth of the DC/DC converter a type-III controller was used:

$$G_C(s) = K\frac{(sT + 1)}{sT} . \frac{(s\alpha/\omega_c + 1)}{\frac{s}{\alpha\omega_c} + 1} . \frac{1}{\frac{s}{\omega_{LPF}} + 1}. \tag{26}$$

The type-III controller consists of a PI controller, defined by K and T, a lead-lag controller, defined by α and ω_c, and a low pass filter with ω_{LPF} as the cut-off frequency. The closed loop system to control the output voltage, according to Fig. 31, is:

$$G_{Cl}(s) = \frac{\widehat{v_o}}{\widehat{v_{ref}}}(s) = \frac{G_C(s)\frac{\widehat{v_o}}{\hat{\phi}}(s)}{1 + G_C(s)\frac{\widehat{v_o}}{\hat{\phi}}(s)} \cong \frac{1}{1 + \frac{s}{Q\omega_f} + \frac{s^2}{{\omega_f}^2}}. \quad (16)$$

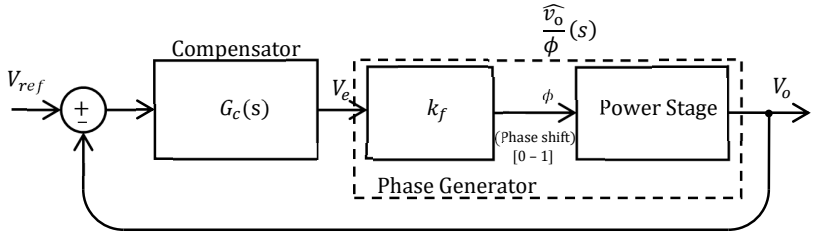


Fig. 31 SM inner control loop.

In our prototype, as an example in order to obtain that transfer function, the controller must have $\omega_c = \omega_0.(1.1)$, $\omega_{LPF} = \pi f_s$ and $\alpha = 2.1$ to have almost 50° of phase margin at around 10kHz and K=1.5 and T=0.0005. This way, the MMC main controller will consider the SM with a simple transfer function and the control dynamics will not be coupled. Fig. 32 shows the SM and the MMC Bode plots.

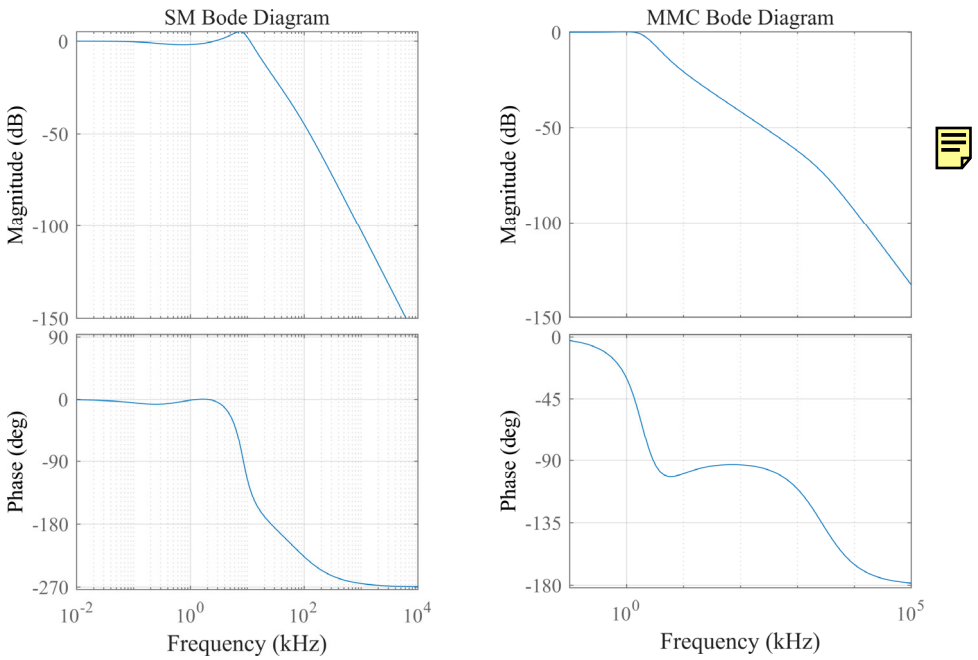


Fig. 32 Closed loop transfer function for: (a) SM using a type-III controller and (b) MMC using a PI controller.

3.2. Proposed MMC with one SC per SM

Fig. 25 presents the proposed MMC-based ESS composed of the SMs in series which work as voltage sources. The proposed topology includes in each SM a bidirectional DC/DC converter with galvanic isolation and a storage device (SC). This allows the discharge current to be perfectly controlled, so the SCs can be balanced using the same DC/DC converter. The DC/DC converter (presented in Section above) is an active-clamped full-bridge with galvanic isolation which allows both power flows for charging and discharging the SC.

Fig. 25 shows two branches of SMs, the top and the bottom. The top branch delivers the positive half sinewave (SM_1-$SM_{N/2}$) and the bottom branch the negative half sinewave ($SM_{N/2+1}$-SM_N). Then, the master controller decides which branch is active.

Thus, the master controller commands each branch to provide or extract power from the load. In addition, an output inductor serves as a filter, as a coupling element to connect the MMC to the grid, and as short circuit protection.

3.2.1. SM Self-balancing technique

Fig. 33.a shows a detailed diagram of one branch. As stated above, there is a master controller which commands all the SMs in the MMC. In order to enable a high voltage output, there are two possible solutions: increase the turns ratio in T_1 (Fig. 26) or add more SMs in series. A disadvantage of the first solution is that the current stress increases in the buck-mode (or delivering mode) affecting the efficiency of the SM and therefore the overall efficiency of the MMC. Therefore, the second solution is more suitable for surpassing high voltage output design requirements.

In a traditional MMC topology adding more SMs would result in a more complex master controller, because of the many signals that are required to sense and control. However, the proposed MMC removes this increased complexity by accommodating a minimal controller in each SM which is in charge of the voltage or current regulation and the self-balancing control.

Fig. 33.b shows the self-balancing controller embedded in each SM. The proposed self-balancing technique is based in the principle of slightly adjusting the power output of the SM, based on the measurements of the adjacent SM SCs' voltages. Thus, if the SC of the SM is under or above the average voltage of the adjacent SMs the power output is adjusted by simply modify V_{REF} or I_{REF} depending on the mode of operation.

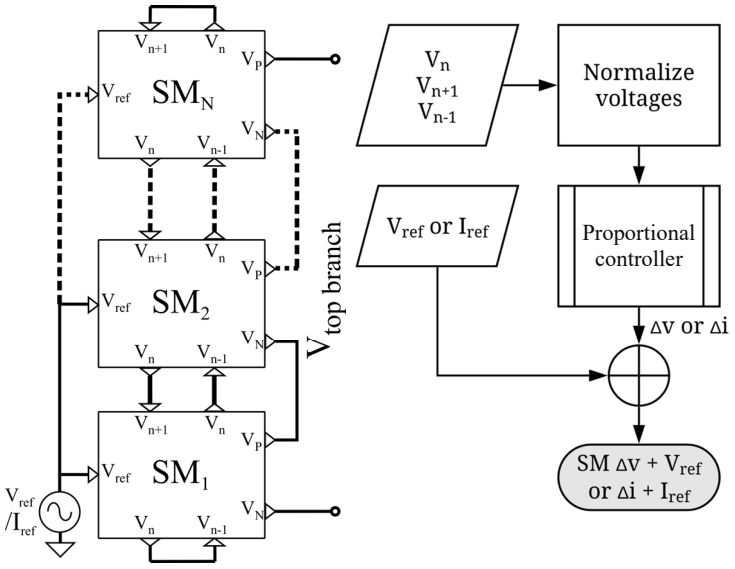
The proposed controller is a proportional controller, this was selected to minimize the computational cost of the controller embedded in the SM, but more sophisticated controls can be implemented if more computational power is available for the SMs. The proportional controller measures the SCs' voltages from the adjacent SMs and its respective SC voltage, therefore an error signal can be defined as:

$$\varepsilon = \frac{3 \cdot V_{SCn}}{V_{SCn+1} + V_{SCn} + V_{SCn-1}} - 1, \tag{27}$$

the reference for the output voltage of the n-th SM when working in the Buck-mode is:

$$V_{REFn} = V_{REF} + \underbrace{V_{REF} K \varepsilon}_{\Delta vn}, \tag{28}$$

or, if the Boost-mode is selected then the same method can be used if a Δi_n is added to I_{REF}. Where K is the proportional gain to limit Δv_n to around 10% of the reference value V_{REF}. This means that Δv_n can be slightly higher or lower than zero, and it is then added to V_{REF}, generating an individual $V_{REFn} = V_{REF} + \Delta v_n$ for the n-th SM. As each SM controller is based on a microcontroller, these calculations are included in the submodules, as Fig. 33 illustrates.



(a) (b)

Fig. 33 MMC (a) branch detailed interconnection, and (b) proportional controller of each SM to achieve the self-balancing capability.

3.2.2. General MMC controller

Fig. 25.b shows two branches of SMs, the top and the bottom. The top branch delivers the positive half sinewave and the bottom branch the negative half sinewave. The master controller needs to sense the output voltage and current of the MMC (v_{MMC} and i_{MMC}) to properly command the whole array of SMs by sending only two variables to each SM. These variables are the operation mode, which can be buck or boost-mode, and V_{REF} (for buck-mode) or I_{REF} (for the boost-mode). These signals are sent to every SM in the corresponding active branch.

To operate in the active power delivering mode (or discharging mode), the main controller sets the operation mode for all the SMs to the buck-mode and the reference of each SM (V_{REF}) to the ESS's required output voltage divided by the number of SMs.

Two reference signals naturally appear from the desired output voltage, $v_{MMC}(t)=V_{MMC}\sin(\omega t+\theta)$, one for the top branch and one for the bottom branch:

$$v_{\mathrm{REF}_{top}} = \begin{cases} \dfrac{V_{\mathrm{MMC}}\sin(\varphi)}{n_{SM}}, if\ 0 < \varphi \leq \pi \\ 0, if\ \pi < \varphi \leq 2\pi \end{cases}, \tag{15.a}$$

and

$$v_{\mathrm{REF}_{bottom}} = \begin{cases} 0, if\ 0 < \varphi \leq \pi \\ -\dfrac{V_{\mathrm{MMC}}\sin(\varphi)}{n_{SM}}, if\ \pi < \varphi \leq 2\pi \end{cases}, \tag{15.b}$$

where n_{SM} is the number of SMs per branch, $\varphi=\omega t+\theta$, V_{MMC} is the output peak value, ω is the frequency in rad/s (grid voltage angular frequency) and θ is the phase shift between $v_{MMC}=V_{MMC}\sin(\varphi)$ and v_{grid}. V_{MMC} and θ can be controlled to deliver active or reactive power like in any DC/AC converter. Thus, all modules together create a sinusoidal waveform.

Fig. 34.a shows a simplified version of the MMC connected to the grid and Fig. 34.b shows the proposed V_{MMC} and θ to deliver active power to the grid and to absorb active power from the grid in the buck-mode. This is possible because of the synchronous rectification described in the previous section, which makes it possible to reverse L_1 current. The upper leg works in the I and II voltage-current quadrants (positive voltage and positive and negative currents) and the bottom leg works in the III and IV voltage-current quadrants (negative voltage, positive and negative currents) imitating the described behavior but with the opposite voltage.

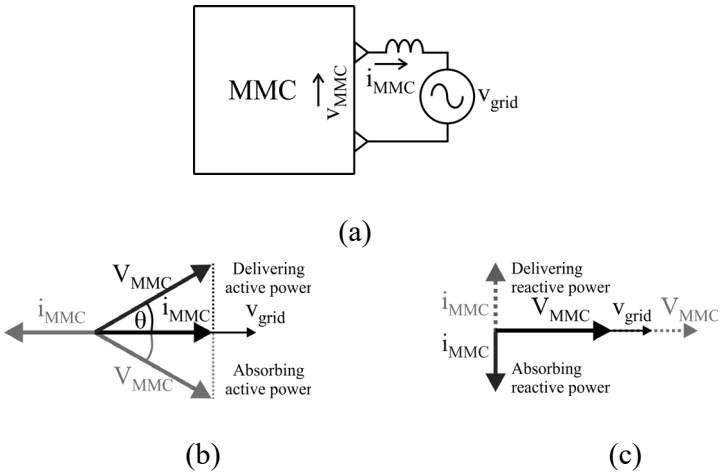


Fig. 34 MMC connected to the grid: (a) basic diagram, (b) phasors when MMC is delivering or absorbing active power, and (c) reactive power.

The converter can deliver and absorb reactive power by increasing or reducing V_{MMC} and by keeping θ equal to zero, as shown in Fig. 34.c. If V_{MMC} is lower than the grid, the reactive power is absorbed and if V_{MMC} is higher, it is delivered. The preferred mode of operation for the SMs is the buck-mode, as it is possible to deactivate Q_c to facilitate negative currents to flow from the grid to the SCs. Therefore, it is possible to command the MMC to lead or lag the grid and also work as a power factor correction unit.

The master controller combines two 180^0 sinusoidal signals to achieve the DC/AC conversion. Fig. 35 shows the controller details. The AC voltage can be directly controlled by using a proportional-resonant (PR) controller [86] or traditional dq-frame PI controllers. In the proposed approach, only the dq-frame method is used.

The phase locked loop (PLL) block obtains the grid angle and frequency [31] and the DC component is obtained using a low pass filter with a cut-off frequency of 5Hz in

order to eliminate a DC component. The dq block includes the low pass filter, the DC signal and the orthogonal signals, so its output are the dq signals and the DC component: dq0 signals.

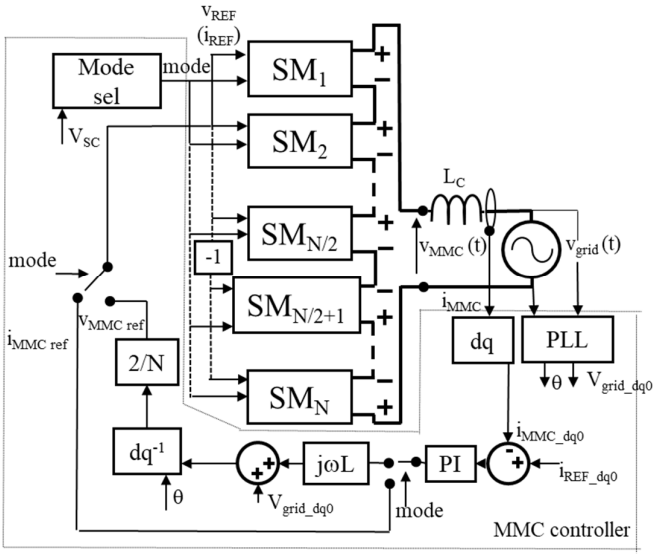


Fig. 35 General MMC controller.

The PI block shown in Fig. 35 consists of three PI controllers: two of them for the dq components and one more for the DC value, which is minimized. The resultant signal is processed and divided by the number of SMs and shifted 180^0 to provide the signals to the lower half of SMs.

In order to absorb power, the SMs are commanded to work in the Boost-mode, and an I_{ref} signal is used to control the amount of power absorbed from the grid. It is preferable to absorb only active power when working in the boost-mode, mainly because in this mode the active clamp cannot be disabled. If the SCs are at a very low voltage (V_{SC}<1.4V), the main controller switches on the boost-mode and each SM works in the boost-mode while the controller governs the grid current. If the SCs reach a sufficiently

high voltage, the SMs can be switched to the buck-mode and work in a voltage-controlled scheme, where the controller supervises v_{MMC} and i_{MMC} (Fig. 34 and Fig. 35) and it is possible to absorb active power by controlling V_{MMC} and θ.

The control diagram of the mode selector is shown in Fig. 36. The mode selector retrieves the SC voltage from one of the SMs (since all of them should be balanced automatically) and check whether the voltage is lower than a predefined value (1.4V in this case). If so, the boost-mode is activated to absorb active power from the grid and recharge the supercapacitors. This voltage is selected in order to charge the SCs when they are close to the lowest limit, where they can no longer deliver charge in the buck-mode. After charging, once they reach a valid working level (2.25V), the master controller switches on the buck-mode, as in this mode it is possible to operate in the four quadrants as described above.

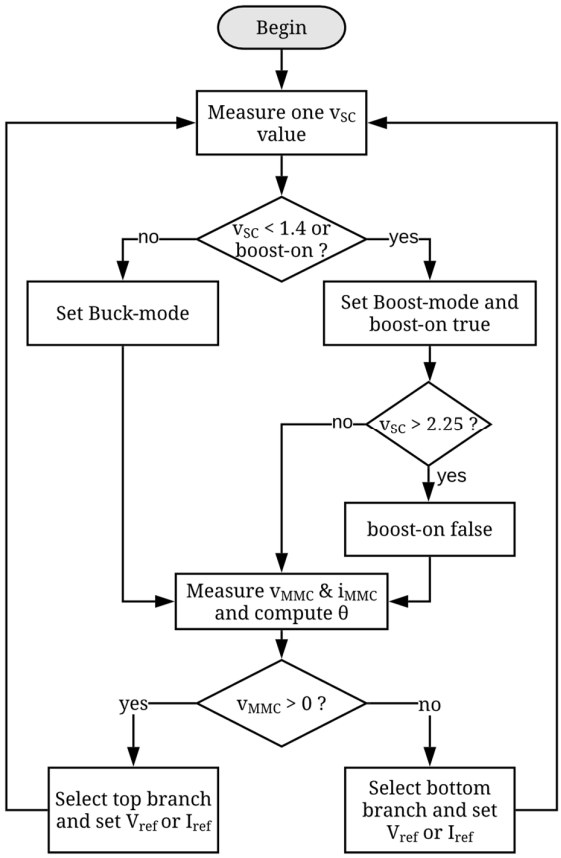


Fig. 36 MMC control diagram for the mode selection.

3.2.3. Simulation results

In order to validate the design, the MMC was simulated using PSIM. Three simulations were performed for a total of 62 SMs, 31 SMs for each branch (top and bottom), to obtain an output voltage of 220VAC at 50Hz. Table 4 shows the components for each SM and the coupling inductor (L_C). In order to reduce simulation time, a SC with a capacitance value of 5F was used.

The first simulation consisted of a discharge process with a forced unbalanced condition in the SCs' voltages to verify the embedded proportional controller working in

the buck-mode. The converter was delivering 10kW to a resistive load. The initial voltage difference was 100mV between the six plotted SC voltages. Fig. 37.a shows the voltage of these six SCs of the whole chain. Notice that at around 0.3 s after the discharging process started, the voltage difference was reduced around 10mV between the maximum and minimum, which is small enough to consider that the SCs are balanced. Although the SCs were initially unbalanced, v_{MMC} stayed stable the entire time while the embedded proportional controller was balancing the SCs. This test also validates the wide input voltage operating range of each SM, from 2.7V to 1.4V. Notice that the voltage output (v_{MMC}) is slightly reduced when SC voltage is lower than 1.5V. In addition, some distortion can be seen in the voltage zero-crossing due to the branch shifting.

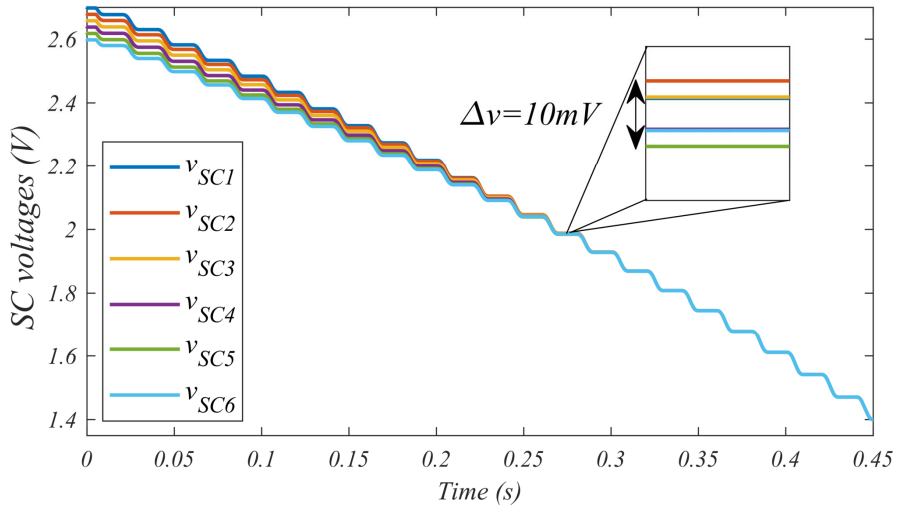
The second simulation consisted of connecting the MMC to the grid in order to validate the 4-quadrant operation in the buck-mode. Fig. 37.b demonstrates the capabilities of the MMC under different angles and amplitudes, as shown Fig. 34.b and Fig. 34.c. In the simulations, the angles and amplitudes were controlled by I_{REF_dq}. Thus, different power transfers are obtained. In order to do that a simulation test bench was created based on Fig. 35.b. Fig. 37.b shows the voltage in two SMs from different half branches (top and bottom), i_{MMC} and v_{MMC}. In the first interval, the MMC delivers 4kVAr of reactive power with I_{REF_dq}=(I_{REF_d}, I_{REF_q})=(0, 25A). Then the MMC absorbs 4kVAr, so I_{REF_dq}=(0, -25A). Then at t=1s, active power is delivered, so for 0.2s the system delivers 4kW-3.2kVAr, I_{REF_dq}=(25A, -20A). After that the reactive current is set to zero and only active power is delivered. Lastly, 4kW of active power is absorbed. This test shows the MMC absorbing and delivering active and reactive power. Notice the balancing

process in the SC voltages and the increase and decrease in SC voltages when absorbing and delivering power, respectively.

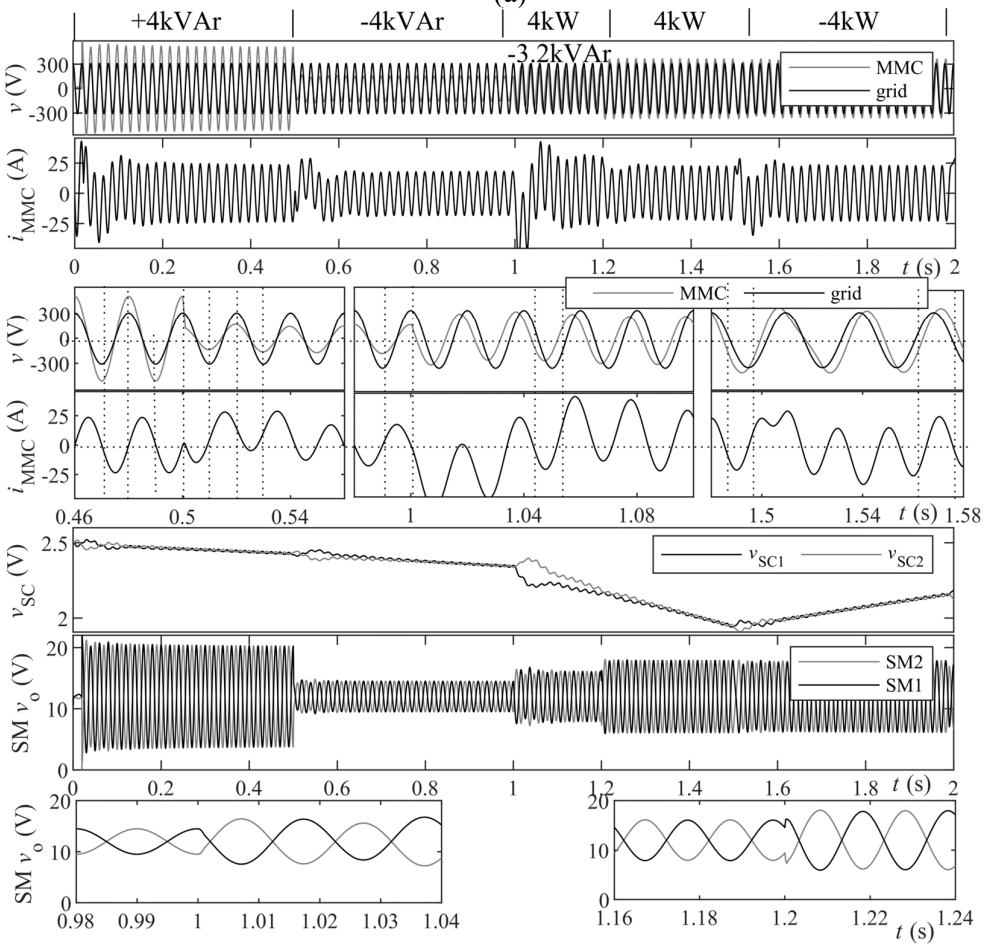
The third simulation (Fig. 37.c) was performed to validate the boost-mode (or absorbing mode), recharging the SC in each SM from 0.75V to 2.25V. This was performed using the test bench of Fig. 35, in boost mode. Then the MMC was commanded to switch to the buck-mode (or delivering mode) and the MMC output voltage, v_{MMC_ref} (t) was controlled to delivered reactive power. Notice that current distortion was augmented when the MMC was delivering reactive power; this is mainly because the SMs turned the active clamp on and off when the current was being absorbed from the grid and delivered to the SCs.

Table 4. Simulation main components

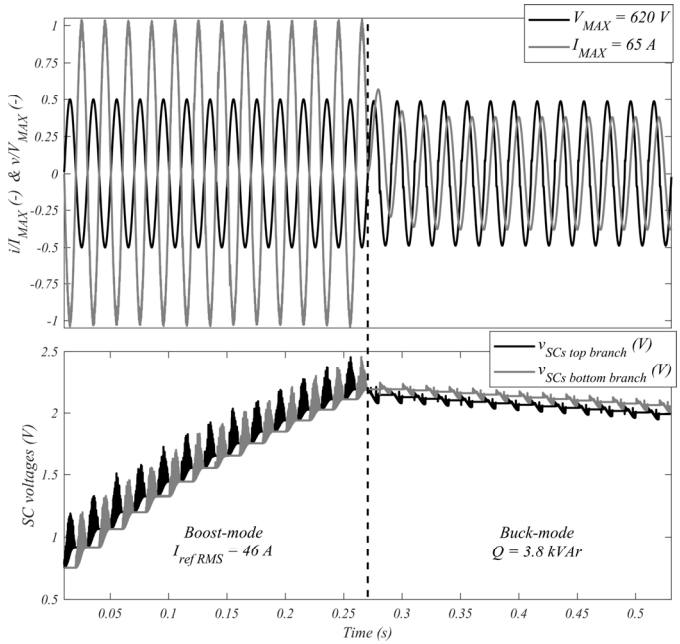
Component	*Value*	*Details*
SC	5F PSIM and 3000F prototype	ESR=0.4mΩ
Q_1 *to* Q_4	3 x BSC009NE2LS5	r_{DS}(on)=0.9mΩ
Q_5 *to* Q_8 *and* Q_c	2 x AON6512	r_{DS}(on)=2.2mΩ
T1 core and L_{MAG}	5.7µH	ELP32, N87 material
Turns ratio	8:1	-
C_C	6 x 0.068µF in parallel	0805 X7R
L1	10µH	EPCOS B82559
C1	2 x 100µF in parallel	Solid tantalum
T_S	10µS	$1/T_S = F_{sw} = 100$ kHz
L_C	500uH	Coupling inductor


SC voltages (V)
Time (s)
Δv=10mV
v_SC1
v_SC2
v_SC3
v_SC4
v_SC5
v_SC6

(a)


+4kVAr
-4kVAr
4kW
4kW
-4kW
-3.2kVAr
MMC
grid
v (V)
i_MMC (A)
t (s)
v_SC (V)
v_SC1
v_SC2
SM v_o (V)
SM2
SM1

(b)

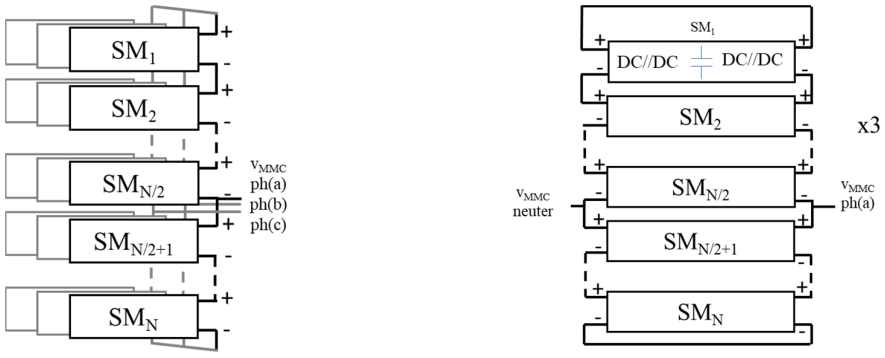


(c)

Fig. 37 Buck-mode: (a) balancing process discharging at 10 kW, (b) delivering or absorbing active or reactive power and (c) changing from boost-mode to buck-mode.

3.3. Extension to three-phase system

The topology can be extended to a three-phase converter by using either a balanced or a non-balanced converter, as Fig. 38 shows. In the balanced converter, all the phases are linked to the ground point and each leg swings from 0V to the maximum voltage as in a traditional. The non-balanced converter requires a module with two DC/DC converters to receive the neuter current or an additional leg.



(a) (b)

Fig. 38 Extension for a three-phase system: (a) balanced and (b) non-balanced.

3.4. Multiple SCs per SM analysis and formulation

The previous subsection validated the proposed MMC-based ESS principles of operation with a single SC per SM. But if more SCs are added in series in each SM for increasing the energy storage capacity or the power rating, a sensitivity analysis to determine the optimal number of SCs per SM is needed. Therefore, this subsection covers in detail the analysis of how many SCs could be placed in series for each SM without creating a too complex SC stack to be balanced. In other words, finding the optimal value of SCs per SM by numerical simulations using Python and Numba. The presented analysis can be also used for adopting the proposed MMC-based ESS for medium-voltage levels.

When the energy source is a single cell, there is no need to internally balance the SC inside the SM, as demonstrated in the previous subsection, it is possible to balance the SCs in the system by simply adjusting the power output of the SMs. However, if more SCs are added in series in each SM in order to increase the efficiency, then it is a must to balance them actively or passively. In this subsection, only the internal active balancing

system is analyzed in order to further increase the efficiency of the ESS. Fig. 39 shows the internal Buck-Boost (BB) balancing system for each SM. As an example, 4 SCs per SM or "Case 4" was used with three buck-boost balancing systems. Therefore, for *N* SCs the required number of balancing systems is (1-*N*).

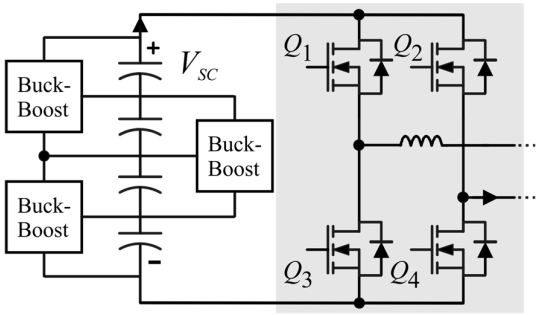


Fig. 39 Internal Buck-Boost balancing system, Case 4 example.

In order to select the optimal number of SCs in series, simulations have been conducted considering the transitors' and diodes' conduction and switching losses, the core and conduction losses of the transformer and the internal buck-boost SC active balancing system used in two or more SCs per SM [13], as they are the principal source of losses.

3.4.1. Sensitivity analysis - methodology

In any design, we need to know:

- the maximum output voltage, $V_{oMAX,}$(V)
- number of supercapacitors (*N*)
- number of supercapacitors per submodule (*M*, or Case).

Then, the total amount of available power can be obtained as $N.P_{MAX\ 1SC}$. This depends on the technology and how we define that power. In general, a good approach is the maximum current which is selected for a certain over temperature multiplied by the minimum voltage which is usually $V_{MAX}/2$. Details can be found in [87].

The analysis of the system will consider a full discharge process, in which all of the losses of the SMs will be included such as: equalizing, switching, conduction, core and copper losses for the components inside the SMs. Fig. 3 shows a brief flow diagram of how a discharging cycle test takes place.

Each SC is initially charged with an unbalanced condition using a uniform distribution of:

$$\bar{V}(0) = [v_1(0), \dots, v_N(0)]^T = Uniform(V_{MAX} - e_V, V_{MAX})^T \in \mathbb{R}^N, \tag{29}$$

the input voltage of the SMs are:

$$\begin{aligned}\bar{V}_{SM}(0) = \big[&v_{1(0)} + v_{2(0)} + \cdots + v_{M(0)}, v_{M+1(0)} + \cdots + v_{2M(0)}, \dots, v_{(N-M+1)(0)} \\ &+ \cdots + v_{N(0)},\big]^T \in \mathbb{R}^M,\end{aligned} \tag{30}$$

considering that a submodule has M SC in series. The nominal capacitance of the N SCs are:

$$\bar{C} = [c_1, \dots, c_N]^T = Uniform\left(C_{NOM} - \frac{e_C}{2}, C_{NOM} + \frac{e_C}{2}\right)^T \in \mathbb{R}^N. \tag{31}$$

Notice that the SC's voltage and capacitance vectors have N-dimension while the module input voltage has M-dimension.

These values are randomized each cycle test. The following step is to calculate the internal BB equalization losses, here the loop algorithm only extracts power from the SC that has more voltage than its pair SC (Fig. 39, arrangement of BBs). After that, the MMC level balancing process takes places, and again, depending on the voltages of the

SCs stacks of adjacent SMs the power output is adjusted accordingly. These balancing steps are done for all the SMs (SM_N) using a counter variable SM_{CNT}. Subsequently, the P_n losses are calculated each time-step, and therefore the efficiency of the system and SMs are recorded through the entire timesteps, allowing to calculate the overall energy efficiency of the MMC and the average efficiency of the SMs for further analysis. The described flow diagram is valid for all Cases, with the exception in Case 1 as there is no necessity for the internal BB process.

The process can be described as:

$$V(t_1) = V(0) + Dt * (I_{SM} + I_{BB}), where$$
$$I_{SM} = [I_{SM1}, I_{SM1}, \dots I_{SM1}, I_{SM2}, \dots, I_{SM2}, \dots, I_{SMM}]^T \in \mathbb{R}^M, \quad (32)$$

meaning that all of the SC in the same SM will have the same current that will be extracted from them (I_{SMn}<0), for example I_{SM1}. And then the next SM will have another current which will be I_{SM2}, until the last SM, which will have $I_{SM\,M}$.

The balancing current, I_{BB} is in general distinct from each other, they are functions of their neighbors:

$$\bar{I}_{BB} = \left[I_{BB12}, I_{BB21} + I_{BB23}, \dots, I_{BBN(N-1)}\right]^T \in \mathbb{R}^M. \quad (33)$$

The relation of these currents is:

$$\sum_{i=2}^{N} I_{BB(i-1)i} = \begin{cases} -\frac{v_2}{v_1}.\frac{I_{BBi(i-1)}}{eff_{BB}}, & if\ V_{i-1} > V_i + DV, \\ -\frac{v_2}{v_1}.\frac{I_{BBi(i-1)}}{eff_{BB}}, & if\ V_i > V_{SC\,i-1} + DV, \\ I_{BBi(i-1)} = 0, & otherwise. \end{cases} \quad (34)$$

The negative current values are constant, $-I_{BB}$, for example I_{BB21} when $v_2 > v_1 + DV$.

The SM power output can be obtained as:

$$P_{O_{SMm}} = eff(V_{SCm}, I_{SCm}).V_{SCm}.I_{SCm}. \tag{35}$$

Thus, the energy losses in a time-step, *dt*, is:

$$E_{LOSS}(k) = \sum_{n=1}^{N} ½ * C_n * {v_n}^2(t_k) - {v_n}^2(t_k + 1) - \sum_{m=1}^{M} P_{O\,SMm}\,. \tag{36}$$

The total losses are:

$$e_{LOSS\,T} = \sum_{k=0}^{K} E_{LOSS}(k)\,. \tag{37}$$

And the total efficiency is:

$$eff_T = \frac{1}{\left[\left(E_{LOSS\,T}/E_{i\,T} - E_{f\,T}\right) + 1\right]}, \tag{38}$$

where:

$$E_{i\,T} - E_{f\,T} = \frac{1}{2}\sum_{n=1}^{N} C_n[{v_n}^2(0) - {v_n}^2(t_k)]\,, \tag{39}$$

this process is repeated step by step until the voltage of the SCs reaches the minimum voltage (t_k=T_K). And then this process is repeated many times using other initial values from the uniform distribution to obtain the distribution function of the losses and the efficiency. Fig. 40 shows a diagram which represents better the sensitivity analysis. This is one experiment and should be repeated *N2* times. After repeating *N2* times, we will have a $\bar{E}_{LOSS\,T} = [e_{LOSS\,T1}, e_{LOSS\,T1}, \dots, e_{LOSS\,T\,N2}]$, which has a mean and a variance, and can be represented using a histogram. Using that vector, confidence interval of minimum efficiency can be achieved to any number of M and N. The key point here, is that efficiencies in the SM will depend on the number of SCs per module due to the proper selection of transistors and transformer design. This is why each Case should be accurately studied in order to obtain a correct efficiency function. As a case study, analyzing a SM built around a SC cell of 3000F is detailed in the next section.

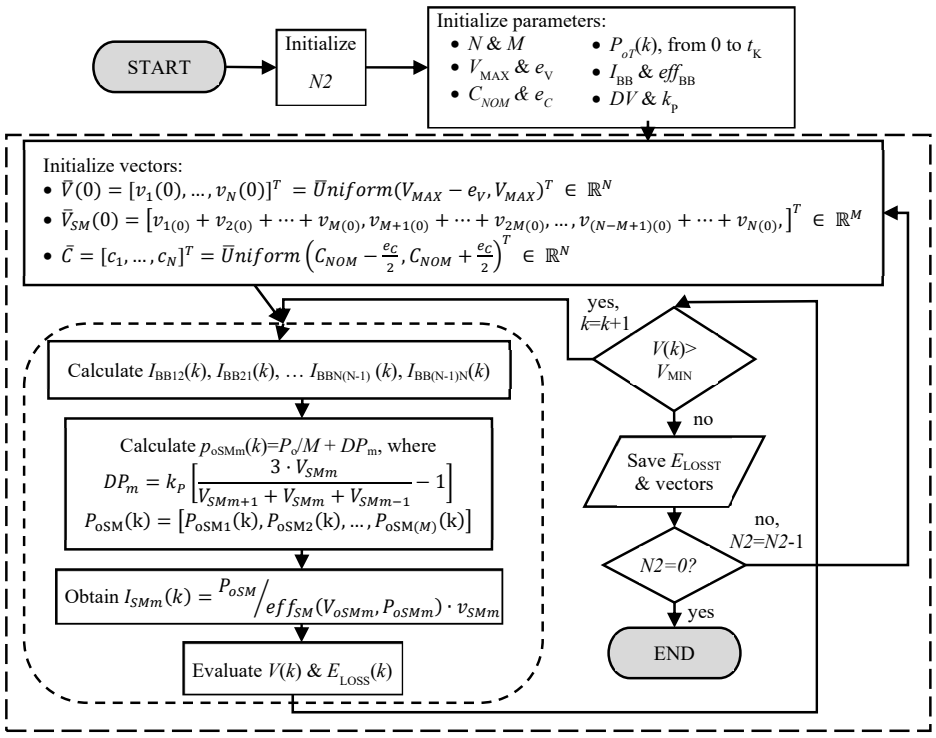


Fig. 40 MMC discharging cycle flow diagram for any Case.

3.4.2. Case study: 3000F SC cell

As a practical example, a single-phase MMC system; composed of N=40 SCs in total at a fixed SC power output of 6.7kW was selected, thus the three-phase system can deliver 20kW. The discharging process considers all the equalizing, switching, conduction, core and copper losses for the components inside the SMs. Fig. 40 shows a brief flow diagram of how a discharging cycle test takes place. Each SC is initially charged with an unbalanced condition of VMAX=2.7 and eV=0.1V with a nominal capacitance value of C_{NOM}=3000F with an error margin of e_C=5%, these values are randomized each cycle test. The following step is to calculate the internal BB equalization losses, here the loop algorithm only extracts power from the SC that has more voltage than its pair SC (Fig. 39, arrangement of BBs). After that, the MMC level balancing

process takes places, and again, depending on the voltages of the SCs stacks of adjacent SMs the power output is adjusted accordingly. These balancing steps are done for all the SMs (SM_M) using a counter variable SM_m. Subsequently, the E_{LOSSn} losses are calculated each time-step, and therefore the efficiency of the system and SMs are recorded through the entire timesteps, allowing to calculate the overall energy efficiency of the MMC and the average efficiency of the SMs for further analysis. The described flow diagram is valid for all Cases, with the exception in Case 1 as there is no necessity for the internal BB process.

The SMs operate at 100kHz switching frequency, this frequency is selected as a good trade-off between size of the DC/DC converter in the SM, the efficiency that can be achieved and the total harmonic distortion if it is used in an AC grid. In addition, with this switching frequency the required number of turns in the primary is equal to  therefore the resulting transformer is easy to prototype and test.

Since the MMC ESS works at 400VDC, with a regulated output voltage of 10V only 40 SMs are needed. This voltage output is selected due the use of 3000F SC cells, which are low voltage energy storage devices and since the DC/DC converter works in the Buck-mode when discharging, if higher voltages are needed the transformer turn-ratio has to be modified, altering the input current peak as well, which could lead to higher conduction losses in the transistors. However, if larger SC modules with higher voltage are used, or if the operating voltage of the ESS must be increased, the SM output voltage can be modified accordingly. Therefore, the transformer turns-ratio is calculated to meet this voltage output requirement.

Since P_{REF} is dependent on the number of SCs in the SM or Case number, the transistors used in the voltage-fed and current-fed sections are selected accordingly to reduce conduction losses and switching losses, as well as the transformer core, which for simplicity and good performance, in all cases an N87 core material is considered. Table 5 summarizes the main selected components:

Table 5. Simulation components of each test case

Case	Voltage-fed MOSFETs	Current-fed MOSFETs	Transformer turn-ratio	Transformer Core
Case 1	5x BSZ014NE2	1x BSC022N04	1:8	ELP32
Case 2	4x BSZ014NE2	2x BSC022N04	1:4	ELP38
Case 3	3x BSZ014NE2	2x BSC022N04	1:3	ELP43
Case 4	3x BSC0501NSI	3x BSC022N04	1:2	ELP58
Case 5	3x BSC0501NSI	3x BSC022N04	1:2	ELP58
Case 6	3x BSC0501NSI	3x BSC022N04	1:2	ELP64
Case 7	3x BSC0501NSI	4x BSC022N04	1:1	ELP64
Case 8	3x BSC022N04	4x BSC022N04	1:1	ELP64
Case 9	3x BSC022N04	4x BSC022N04	1:1	ELP64
Case 10	3x BSC022N04	4x BSC022N04	1:1	ELP64
Case 11	4x BSC022N04	4x BSC022N04	1:1	ELP64

In order to reduce simulation time, a fixed time step of one second is used, and the self-balancing error algorithm is tuned taking into consideration the relatively large time step, which operates by slightly increasing the output power of the SM if the SCs have higher voltage than the adjacent SMs SCs' voltage, or vice versa if the SCs' voltage is lower, therefore the Power ($P_{\mathrm{oSMm}}(k)$) extraction can be calculated as in Fig. 40, in which the adjust constant ($k_P = 15{,}000$) is used.

Thus, the controller is a simple proportional controller with a gain of k_P. However, ΔP is limited to 10% P_{MAX} in order to avoid large and unrealistic SM output voltage changes.

For the internal buck-boost active balancing system the operating power is fixed at 15W with an efficiency of 70%. These values are selected using [12, eq(12)], since

most commercial SCs from the same batch are well within the 7.5% of capacitance change and because the internal balancing system operates from 1.35 to 2.7V range.

As described in Fig. 40, the equalization is done at the start of each time step, before the SM is discharged with the calculated MMC level P_{oSM}. Since the internal BB can overshoot due the relatively large time step used in the simulations, a DV of 20mV is introduced to avoid voltage ripple. Therefore, the internal BB balancing process loop operates as expressed in (34).

3.4.3. Results of the analysis

For analyzing all the cases, multiple tests were performed in several the cases, in all the cases 10,000 different initial v_{SC} and C_{SC} conditions using uniform distributions around the mean value and considering the parameters' tolerances were tested.

The first test validates that in each Case is balancing all the SCs properly. The second test is a probabilistic analysis for 10,000 different simulations for each case. The results for the second test are shown in the form of histogram and a Cumulative Distribution Function (CDF) plot which illustrate the efficiency of each SM through all the time steps. Finally, the last test focuses on the efficiency of the energy transferred for the complete system, again 10,000 different simulations were evaluated for each case and the results are shown in the histogram and CDF plot forms.

3.4.3.1. MMC self-balance and internal BB equalization test.

The first simulation validates the MMC self-balancing capabilities for all the Cases; and from Case 2 to the subsequent Cases, the internal buck-boost active balancing system is used and validated as well.

Case 1 balances the SCs in only 15 seconds since only the self-balancing algorithm (included in the SMs) is working and there is no internal buck-boost balancer because only a single SC is contained in each SM. Therefore, there is no limitation for Case 1 in terms of balancing power. Fig. 41.a shows the resulting voltage plot for Case 1.

In Case 4, the internal buck-boost active balancing system have a fixed operating power of 15W with the described efficiency of 70%. Fig. 41.b shows the resulting voltage plot for each SC in the MMC system for Case 4.

Fig. 41.c shows a scattered surface plot between the initial SCs voltage error V_{err} (y-axis) and the final error once the discharge process is done (x-axis), for Cases 1, 4 and 9. Illustrating how well the equalization is done in each case. Since Case 1 does not use the internal BB equalizer the balancing is more accurate and has less dispersion for the 10,000 simulations. Once the internal BB is used and the number of SCs per SM increases and the dispersion increases as well. This is due the fact that in some simulations it might happen that the SCs' voltages are distributed in such way that there is one SC relatively lower than the SCs in the same stack, but the SM voltage is higher than its adjacent SMs. Therefore, for those scattered conditions it might need an additional charge-discharge cycle to reach adequate balancing levels. However, based on these results we can observe that even for Case 9 the peak of the Gaussian bell is at 60mV, which is considered a small balancing error. This test validates the self-balancing operation of the SM and the internal active balancing system at the proposed power.

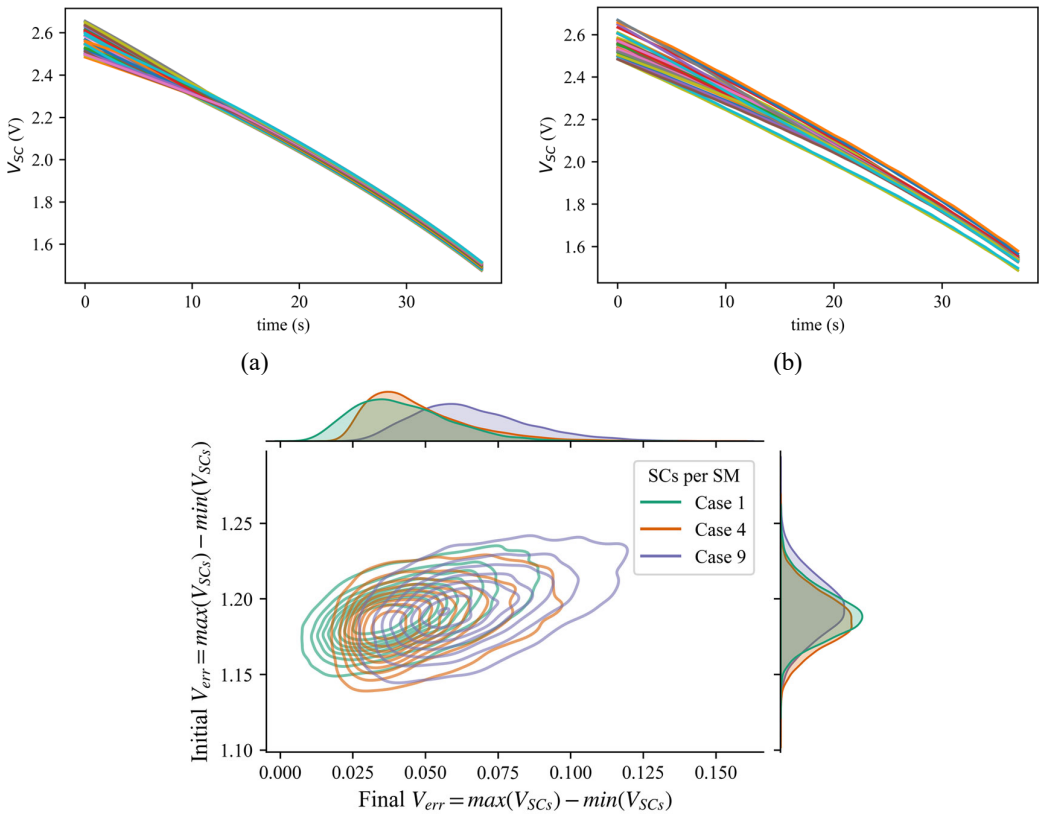


Fig. 41 Voltage plot of each SC for the discharging cycle for (a) Case 1, (b) Case 4 and (c) scattered surface plot for Case 1, 4 and 9.

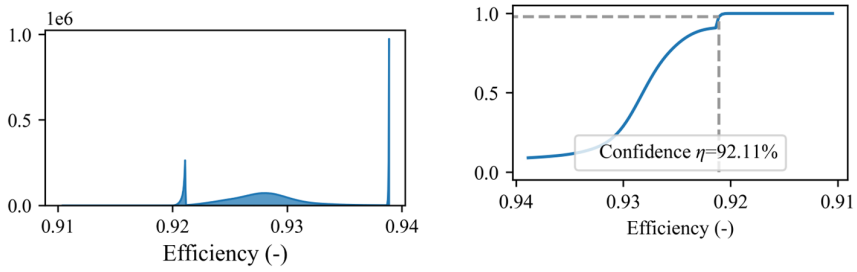
3.4.3.2. SMs' efficiency through the entire discharge.

The second test is focused on a probabilistic study for a point of view of the SMs efficiency through the entire duration of the discharge, which is done by reproducing 10,000 discharge tests varying the initial SCs' voltage and capacitance and recording the efficiency of the SMs in each time step.

The confidence analysis considers extracting the efficiencies of the SMs during the whole discharge and build the histogram for each Case. After the histograms are built, the Cumulative Distribution Function (CDF) is generated.

Fig. 42 shows the SMs' efficiency histograms and the CDF for Case 1, 4 and 9. Notice that in Case 1, there are a maximum and minimum peak, those peaks are produced when the MMC self-balancing is working at its maximum and minimum error respectively (since ΔP is limited to 10% P_{MAX}). For Case 4 there are four clearly distinct sets of efficiency in the histogram, the set from the left appears because all the internal Buck-Boost active balancers are working. The next peak is because one of those internal Buck-Boost is not active, and the others two peaks are because only two balancers and one balancer are working respectively. The same behavior happens in Case 9, but now all the sets have overlapped each other.

From the point of view of reliability, the CDF plots present which is the probability to have an efficiency higher than a certain limit. From the point of view of the design, it is useful to indicate that the efficiency is higher than a certain level. Fig. 5 shows exactly this with dashed lines, with an efficiency confidence level of 95%. For Case 1 (Fig. 42.a) the efficiency (η) is 92.11%, for Case 4 is 93.54% (Fig. 42.b) and for Case 9 is 91.06% (Fig. 42.c), all of them with 95% confidence level.



(a)

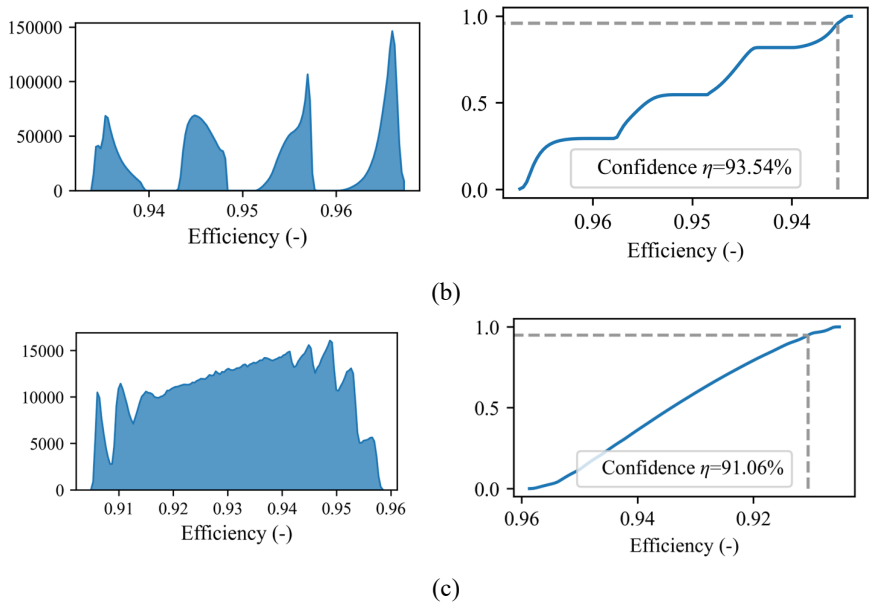


Fig. 42 SM efficiency histograms and CDF plots for Case 1, 4 and 9.

These obtained confidence values of efficiency are then plotted for each Case as shown in Fig. 43. Furthermore, to better illustrate the impact of increasing the number of SCs per SM when there is an unbalance condition in the efficiency of the SMs, both balanced and unbalanced conditions were tested. However, the same approach of randomizing the *C* value for each SM is still conserved in both situations. Thus, when the internal balancing system must work and interact with the MMC balancing method, the efficiency is reduced. In practical applications, the efficiency will be much closer to the balanced (blue) one, as the system is balancing the cells all the time.

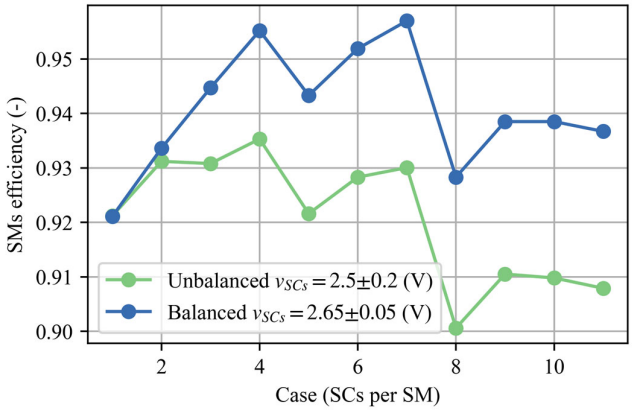


Fig. 43 Minimum SMs efficiency with a confidence level of 95% for unbalanced and balanced initial conditions for all Cases.

3.4.3.3. MMC overall efficiency.

For the third test, the efficiency of a complete discharge cycle is calculated by taking the output energy of the complete MMC ESS divided by the initial energy contained in all the SCs. The result has a normal distribution as Fig. 44 shows for the different cases. Based on this test we can obtain the efficiency of the complete ESS, for the different cases for any SC parameter dispersion, including any confidence level.

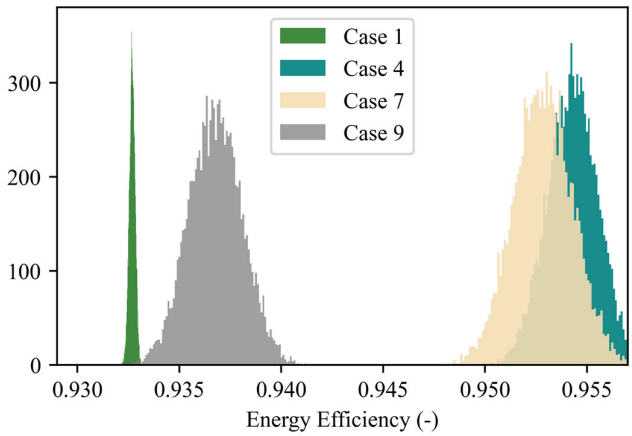


Fig. 44 Energy efficiency histograms for Case 1, 4 and 9.

These obtained MMC ESS energy efficiency values are then plotted for each case as shown in Fig. 45 with a confidence level of 95%. Again, both balanced and unbalanced conditions were tested, the randomized *C* percentage remains the same for both tests.

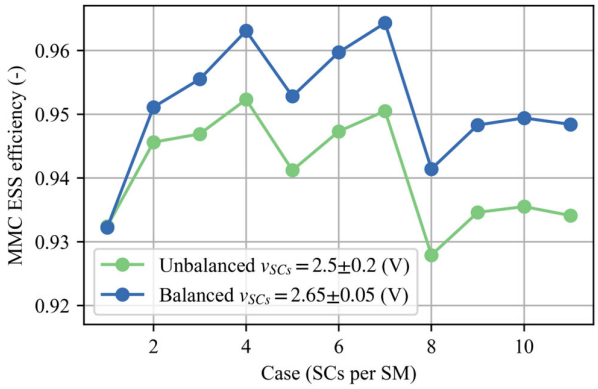


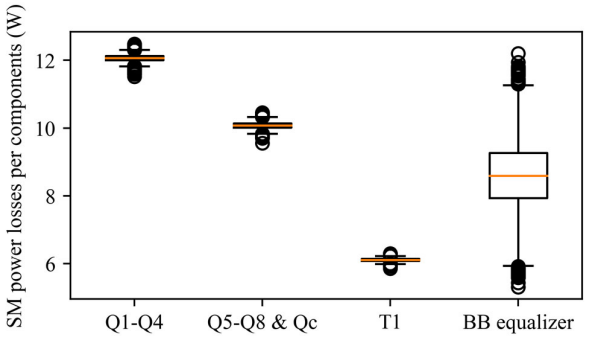
Fig. 45 CDF Energy Efficiency plot for (a) unbalanced and (b) balanced initial conditions for all Cases.

From these simulations we can conclude that Case 4 and Case 7 are the best performing, with an efficiency of around 95.3%. Therefore, if we compare these results with Case 1, an increase of 2.4% in the efficiency can be achieved by properly selecting the number of SCs per SM. The confidence analysis also validates that the efficiency increase is guaranteed even if the SCs' capacitance changes over time or if there is an abrupt charge/discharge cycle that could cause a major unbalance between the SCs. The same probabilistic analysis can be done for different initial conditions or to test a different ESS setup. The key aspect is that the modeled system can be tested several times to address all possible scenarios and select the desired confidence level.

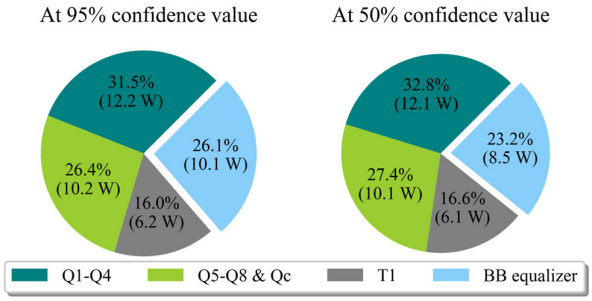
Therefore, although Case 7 is slightly better, the increased complexity for each SM is taken into account and for this reason, Case 4 is selected for reproducing the simulation results in a small-scale prototype which will be discussed in the following section.

Finally, to conclude this section, an analysis of power losses per component was done in Case 4 to illustrate how the SMs behave with different initial conditions. Again, the same parameters from the previous tests were used to represent the main component losses for a complete discharge cycle for 10,000 times. Fig. 46.a shows the box plot for each set of main components analyzed per SM (see Table 5), and Fig. 46.b the pie charts for confidence values of 95% and 50%. For Q_1-Q_4 the 95% of the losses stays below 12.21W, being in their majority conduction losses. For Q_5-Q_8 & Q_c the 95% of the values stays below 10.22W, again, since some switching intervals occur at zero current and zero voltage switching the losses come from the r_{DS}(ON) resistance of the MOSFETs. For T_1 the main source of losses are the copper losses, and they minimally shift away from the 6.26W value. For the Buck-Boost (BB) internal equalizer the 95% of the values are contained within 10.15W. Notice how the components used for the DC/DC converter are well contained into a small section of the box plot, indicating that the MMC self-balancing technique is not contributing to major losses. However, for the internal Buck-Boost there is wide region of losses, and this can be explained by how the equalization is done by transferring energy from one SC to the next with a fixed efficiency of 70%.

Thus, in order to increase furthermore the efficiency, efforts can be focused on the internal balancing system and eventually in Q1-Q4 transistors.



(a)



(b)

Fig. 46 SM power losses for the main components (a) box plot and (b) pie charts at 95% and 50% confidence levels.

4. Experimental results and validations

From the previous section two prototypes where built, the first one was done before the sensibility analysis to validate the operation of the Proposed ESS; therefore, efficiency was not high and for these reasons the sensibility analysis was carried out in order to improve and analyze the system's efficiency. This section shows the relevant tests done for both prototypes and the validations test benches for them.

4.1. Prototype with a single SC per SM

The first prototype consisted of two SMs for each half branch was constructed, with a maximum power transfer of 175W per SM and only one SC in each SM. Fig. 47 shows the complete MMC, composed of the top branch, the bottom branch, a v_{MMC} and i_{MMC} sensor board and a microcontroller unit (MCU), which acts as master controller. Each SM integrates all the components listed in Table 4, power switches are at the bottom and attached to a heatsink large enough to maintain operating temperatures within a safe margin using natural convection. In addition, the TI TMS320F28027 DSP was used as the SM controller, which includes the proportional controller for balancing the SCs and the PWM generator. The SM planar transformer was designed and developed specially for the prototype using an interleaving scheme with custom built windings [88]. The master controller was implemented in a Texas Instruments Delfino F28379D MCU, which measures and gives the references to the SMs.

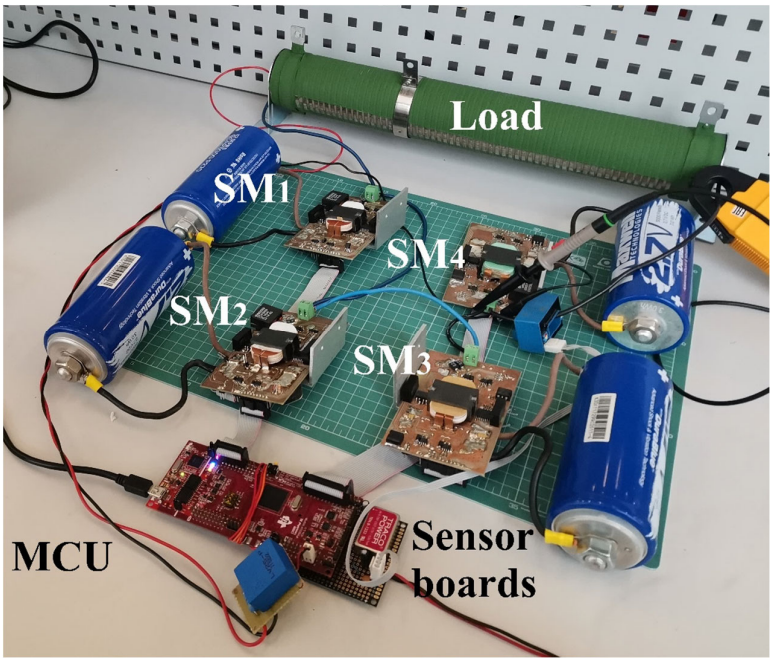
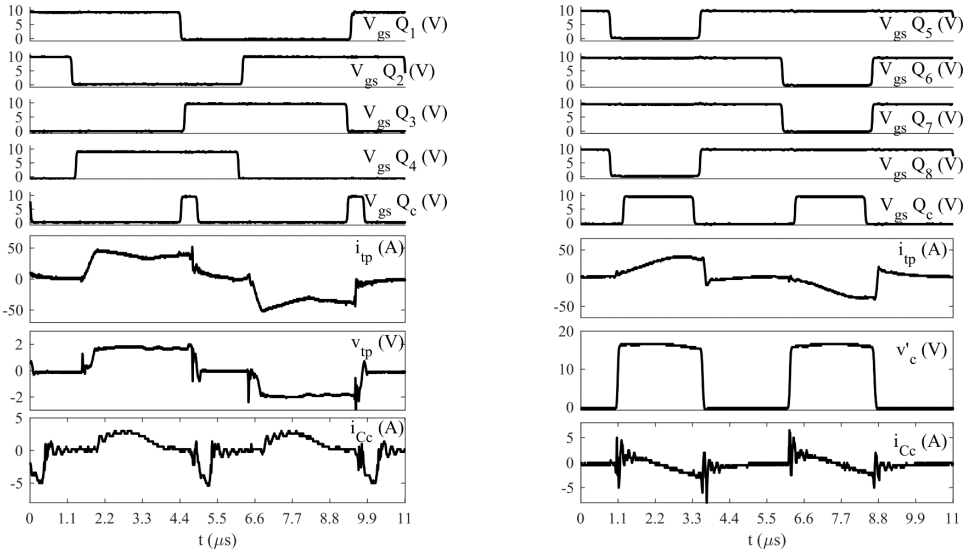


Fig. 47 Complete MMC Prototype.

Four experimental tests were performed. The first test was the validation of the SM waveforms in buck-mode and boost-mode as Fig. 48 shows. These waveforms are consistent with the theoretical and simulated ones (Fig. 28 and Fig. 29).



(a) (b)

Fig. 48 Experimental waveforms for each SM in (a) buck and (b) boost-mode.

The second test shows the operation of the MMC. Fig. 49 shows the discharge mode (buck-mode) with a resistive load; the test depicts the MMC output voltage and current (v_{MMC} and i_{MMC}). It shows that the voltage stayed stable during a step change in the load.

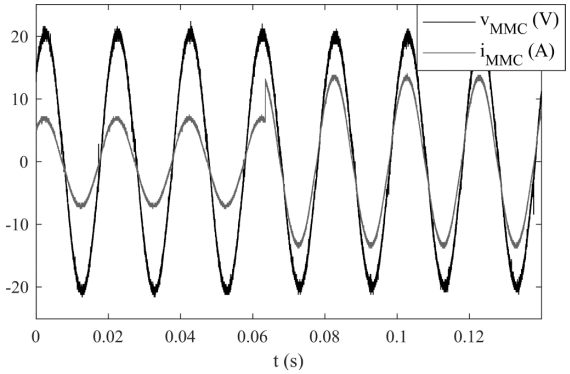
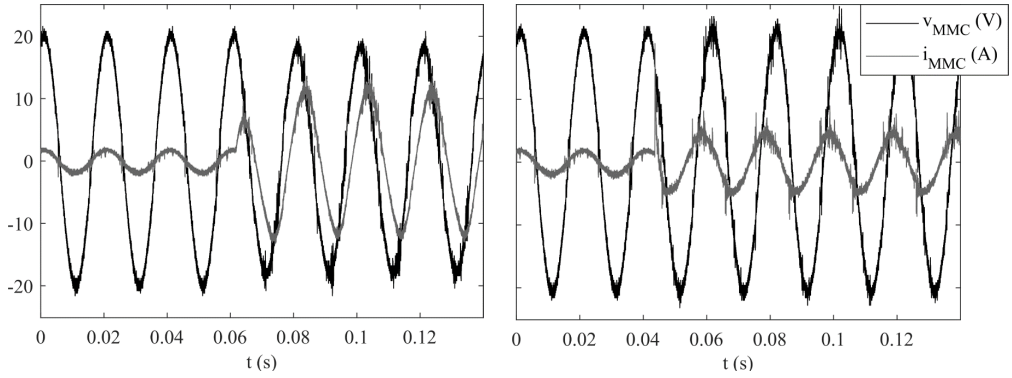


Fig. 49 MMC output voltage and current for a step change in the load.

The third test shows the operation of the MMC when the load changes from R to RL and from R to RC as Fig. 50 shows, which validates the operation with reactive current flow. As the grid connection was validated in the simulation section, in the experimental results the MMC was only tested using different passive loads, and thus the MMC was the only AC grid generator.

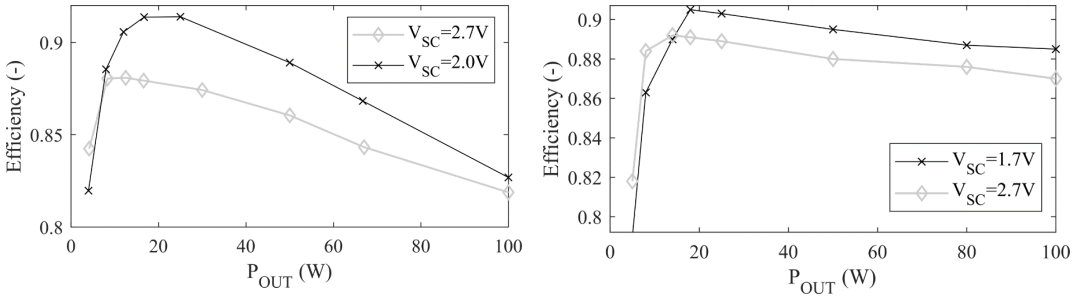


(a) (b)

Fig. 50 Step response from (a) R to RL and (b) R to RC.

Finally, the fourth test shows the efficiency of the whole MMC in both operation modes at different output powers and with two different SC voltages as Fig. 51 shows. The efficiency at high power is not as high as in a high voltage DC/DC converter because

of the large currents and low input voltages; however, it can be improved by paralleling DC/DC converters in each submodule and by using wide band semiconductors, such as GaN or SiC. The prototype shows how the circuit works; however, the efficiency is not optimized and can be further improved.



(a) (b)

Fig. 51 Efficiency of the MMC for (a) buck and (b) boost-mode.

This prototype validates the principles of operation for the proposed MMC-based ESS with the self-balancing technique. Allowing to use the SMs with integrated energy storage devices such as SCs or batteries to create a more flexible ESS, in which is possible to increase the capacity or the power ratings by adding more SMs in series. The complexity for expanding the number of SMs of other MMCs found in the literature review is avoided by having the self-balancing algorithm embedded in each SM. With the self-balancing algorithm it is also possible to avoid recirculating currents between the SCs, hence less energy losses occur due the active balancing system, since each SM delivers the required amount of power for reaching the equalized steady state.

4.2. Prototype with 4 SCs per SM obtained after the sensitivity analysis

Based on the sensitivity analysis done in Section 3.4, and with the validations done for the AC operation, this subsection validates the efficiency gains by using 4 SCs per SM.

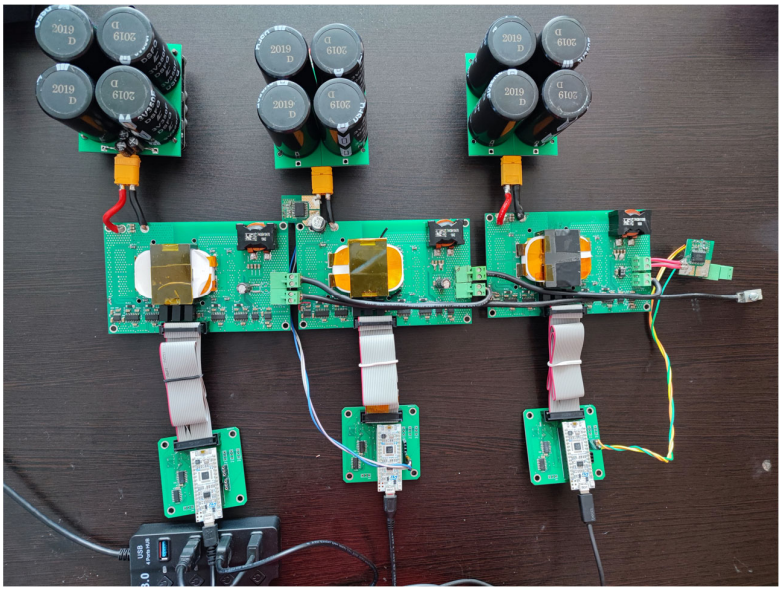
In order to have a reliable information about the losses in the modules and balancing systems, a prototype of the MMC with three SM was built. Fig. 52.a shows the prototype, where three "Case 4" SMs are connected. The characteristics of each SM with an efficiency of ~94% is presented in Table 6.

Table 6. Experimental validation SM components

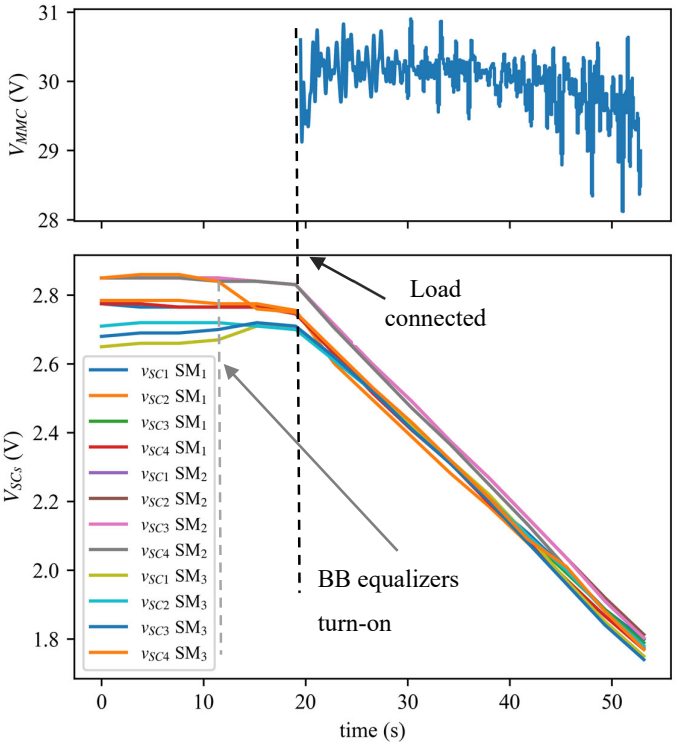
Item	Model	Description
Q_1-Q_4	3x BSC0501NSI	30 V_{DS} 1.9mΩ, Q_g = 24nC
Q_5-Q_8, Q_c	3x BSC022N04	40 V_{DS} 2.2mΩ, Q_g = 28nC
SC stack	4x DSF357Q3R0	350F 3.0V 3.5mΩ Supercapacitor
T_1 Core	B66291G0000X197	ELP 43/10/28 N97 7500nH
L_1	74436410150	Wurth 1.5uH 1.31mΩ I_{SAT}=110A
MCU	NUCLEO-L412KB	ARM STM32 80MHz with FPU
Q_1-Q_8 Driver	4x SI8275AB	Dual-channel isolated MOSFET Driver
Q_c Driver	Si8271GBD	Isolated MOSFET Driver
V_{SC}, V_O sensor	ADUM3190AR	Isolated operational amplifier
Current sensor	MCR1101-50-3	Bidirectional 50A, 1.5MHz BW

Case 4 was selected as the optimal solution, for that a discharge cycle in a three SM configuration for the ESS was performed. Fig. 52.b shows waveforms of the systems during the discharge process, validating the internal BB balancing and the MMC level balancing operation. The internal BB equalizers are turned on at second 11, achieving very fast balancing for each SM. Once the load was connected, the MMC level balancing algorithm started to operate and the voltage error between each SC from different SMs

started to decrease, and by the end the difference between max(v_{SCs})-min(v_{SCs}) was lower than 80mV, which can be reduced further if a better isolated operational amplifier is used.



(a)



(b)

Fig. 52 MMC (a) prototype with Case 3 SMs and (b) discharge process using initial unbalanced conditions.

Efficiency tests were run at different power at the nominal output voltage per SM, this test validates the theoretical losses calculated for the Case number, and therefore for the other Cases as well. Fig. 53 shows the efficiency of the SM at different power levels and the theoretical curve obtained from the numerical simulations.

The balancing system was also tested for evaluating its losses, in this case a charge-discharge cycle was performed with different initial voltages in the SCs, and the efficiency of balancing was evaluating considering the energy delivered from the SCs and the energy received by the load. The efficiency of the balancing system can be assumed to be fixed at ~70% efficiency, which was the value used in the simulations. Using Fig. 53 plots, a mathematical model, with a polynomial approximation with R^2=0.973, was performed and then used in the probabilistic analysis to compare the analysis with the simulation experiments in Case 4. The plot in Fig. 54 should be compared with the plots in Fig. 44 and Fig. 45 for Case 4. Thus, the expectation was 95% and the experiments show 93%, mainly due to the 2% efficiency difference in the SM converter.

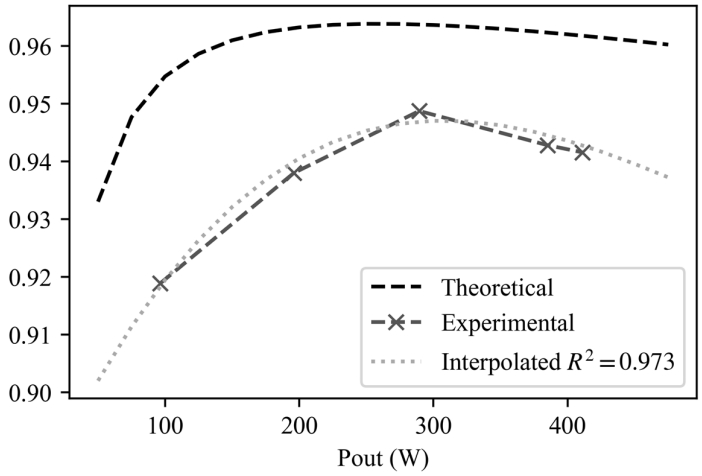
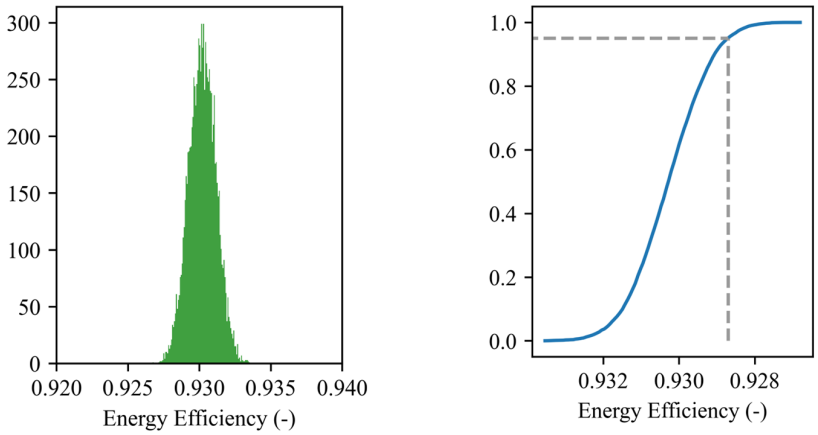


Fig. 53 SM obtained efficiency values vs theoretical curve.



(a) (b)

Fig. 54 Probabilistic study based on the extracted SM efficiency from the prototype, (a) histogram and (b) CDF plot.

5. Conclusions and future work

The main contributions of this thesis work are the formulation of an MMC-based ESS and the methodology for assessing the losses presented in such type of ESSs. In a traditional supercapacitor ESS, four stages are needed: energy storage devices, the

balancing system, and the DC/DC and DC/AC converters that connect the storage devices to the grid. The SC ESS that is proposed uses a modular multilevel converter (MMC) that is able to reduce the number of stages by performing the self-balancing process and the DC/DC and DC/AC conversions in a single stage.

Each submodule (SM) of the MMC consists of a DC/DC converter and a single SC or a SC stack. The DC/DC converter is a bidirectional full-bridge that has an active clamp and soft-switching techniques and works at 100 kHz and at low input voltages. In addition, the DC/DC converter includes a planar transformer, galvanic isolation is also achieved, and a bulky 50Hz transformer can be avoided.

The MMC can be implemented using a large number of SMs in series without increasing the complexity of the main controller. This is because the balancing process is performed in each SM, and the main controller only governs the power flow between the SCs and the grid. This makes the MMC attractive for SC-based ESS designs. The design was validated in simulations and in a real prototype. Four-quadrant operation with low distortion was achieved.

Once the proposed MMC design was validated, a methodology for assessing its performance and improving the efficiency was analyzed. This formulation was done by describing the power losses in a system of N number of SCs and an M number of SMs and then, running numerical simulations to carry out a probabilistic analysis. This probabilistic analysis is key to determine the proper number of SCs in the SM for reducing the losses and therefore improving the efficiency of the system. With the proposed methodology, a 400VDC ESS was studied in detail. The analysis showed that the best-performing number of SCs for each submodule is Case 4. This provides the best efficiency

for initially unbalanced and balanced conditions. The study describes in detail the case study to guarantee the efficiency by performing a sensitivity analysis from 10,000 tests with uniform random values of capacitance and initial voltages for the SCs. The same analysis can be done for any specific voltage and number of SCs.

The simulation results from the probabilistic analysis are based on real data and are validated through a small-scale prototype for the optimal number of SCs in a submodule. In the tests, the SCs have intentionally different capacitance values as well as initial voltage conditions. The efficiencies obtained in the experimental results are consistent with the sensitivity analysis, validating the proposed methodology and the MMC-based ESS.

Since the future grid must be ready for further integration of renewable energy, the increased efficiency of the MMC-based ESS is an attractive solution to sustain the grid operation. As the MMC-based ESS is flexible in terms of power and energy capacity, it allows a rapid implementation and a seamless expansion in the future.

Future work should concentrate on correctly sizing the ESS for interconnecting to the grid and responding to abrupt changes in power and therefore sustaining the renewable energy injection, as well as developing a proper strategy to manage the SCs cells and extend their lifetime. Also, since the internal balancing system is the main source of energy losses when more than 1 SCs are present in each SM, it is necessary to integrate the internal balancing system in a single stage too. For some other applications, such as vehicular, UPS/off-grid or large bulk electricity storage, a hybrid ESS can be more convenient. Therefore, it will be needed to analyze the integration of two or more energy storage devices at the submodule level.

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